ON Semiconductor

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NCL30000

Power Factor Corrected Dimmable LED Driver

The NCL30000 is a switch mode power supply controller intended for low to medium power single stage power factor (PF) corrected LED Drivers. The device is designed to operate in critical conduction mode (CrM) and is suitable for flyback as well as buck topologies. Constant on time CrM operation is particularly suited for isolated flyback LED applications as the control scheme is straightforward and very high efficiency can be achieved even at low power levels. These are important in LED lighting to comply with regulatory requirements and meet overall system luminous efficacy requirements. In CrM, the switching frequency will vary with line and load and switching losses are low as recovery losses in the output rectifier are negligible since the current goes to zero prior to reactivating the main MOSFET switch.

The device features a programmable on time limiter, zero current detect sense block, gate driver, trans-conductance error amplifier as well as all PWM control circuitry and protection functions required to implement a CrM switch mode power supply. Moreover, for high efficiency, the device features low startup current enabling fast, low loss charging of the V_{CC} capacitor. The current sense protection threshold has been set at 500 mV to minimize power dissipation in the external sense resistor. To support the environmental operation range of Solid State Lighting, the device is specified across a wide junction temperature range of −40°C to 125°C.

Features

- Very Low 24 μA Typical Startup Current
- Constant On Time PWM Control
- Cycle-by-Cycle Current Protection
- Low Current Sense Threshold of 500 mV
- Low 2 mA Typical Operating Current
- Source 500 mA/Sink 800 mA Totem Pole Gate Driver
- Reference Design for TRIAC and Trailing Edge Line Dimmers
- Wide Operating Temperature Range
- No Input Voltage Sensing Requirement
- Enable Function and Overvoltage Protection
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- LED Driver Power Supplies
- LED Based Down Lights
- Commercial and Residential LED Fixtures
- TRIAC Dimmable LED Based PAR Lamps
- Power Factor Corrected Constant Voltage Supplies

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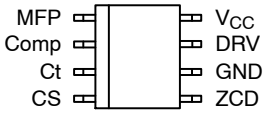
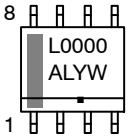
SOIC−8
CASE 751

PIN CONNECTION



(Top View)

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCL30000DR2G	SOIC−8 (Pb−Free)	2,500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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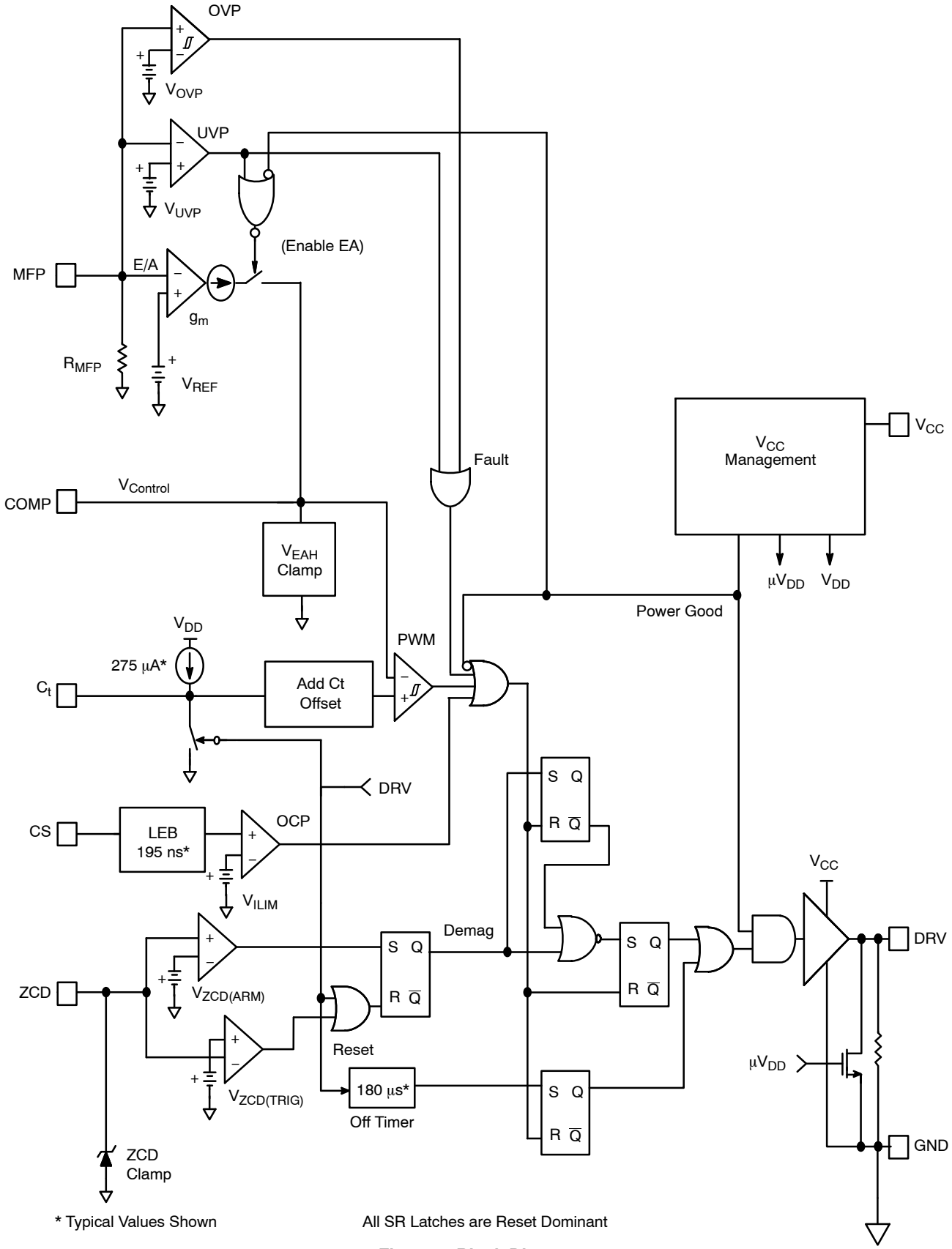

Figure 1. Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Function
1	MFP	The multi-function pin is connected to the internal error amplifier. By pulling this pin below the V_{uvp} threshold, the controller is disabled. In addition, this pin also has an over voltage comparator which will disable the controller in the event of a fault.
2	COMP	The COMP pin is the output of the internal error amplifier. A compensation network is connected between this pin and ground to set the loop bandwidth. Normally this bandwidth is set at a low frequency (typically 10 Hz – 20 Hz) to achieve high power factor and low total harmonic distortion (THD).
3	C_t	The C_t pin sources a regulated current to charge an external timing capacitor. The PWM circuit controls the power switch on time by comparing the C_t voltage to an internal voltage derived from $V_{Control}$. The C_T pin discharges the external timing capacitor at the end of the on time cycle.
4	CS	The CS input is used to sense the instantaneous switch current in the external MOSFET. This signal is filtered by an internal leading edge blanking circuit.
5	ZCD	The voltage of an auxiliary zero current detection winding is sensed at this pin. When the ZCD control block circuit detects that the winding has been demagnetized, a control signal is sent to the gate drive block to turn on the external MOSFET.
6	GND	This is the analog ground for the device. All bypassing components should be connected to the GND pin with a short trace length.
7	DRV	The high current capability of the totem pole gate drive (+0.5/−0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs. The driver stage provides both passive and active pull down circuits that force the output to a voltage less than the turn-on threshold voltage of the power MOSFET when $V_{CC(on)}$ is not reached.
8	V_{CC}	This pin is the positive supply of the controller. The circuit starts to operate when V_{CC} exceeds $V_{CC(on)}$, nominally 12 V and turns off when V_{CC} goes below $V_{CC(off)}$, typically 9.5 V. After startup, the operating range is 10.2 V up to 20 V.

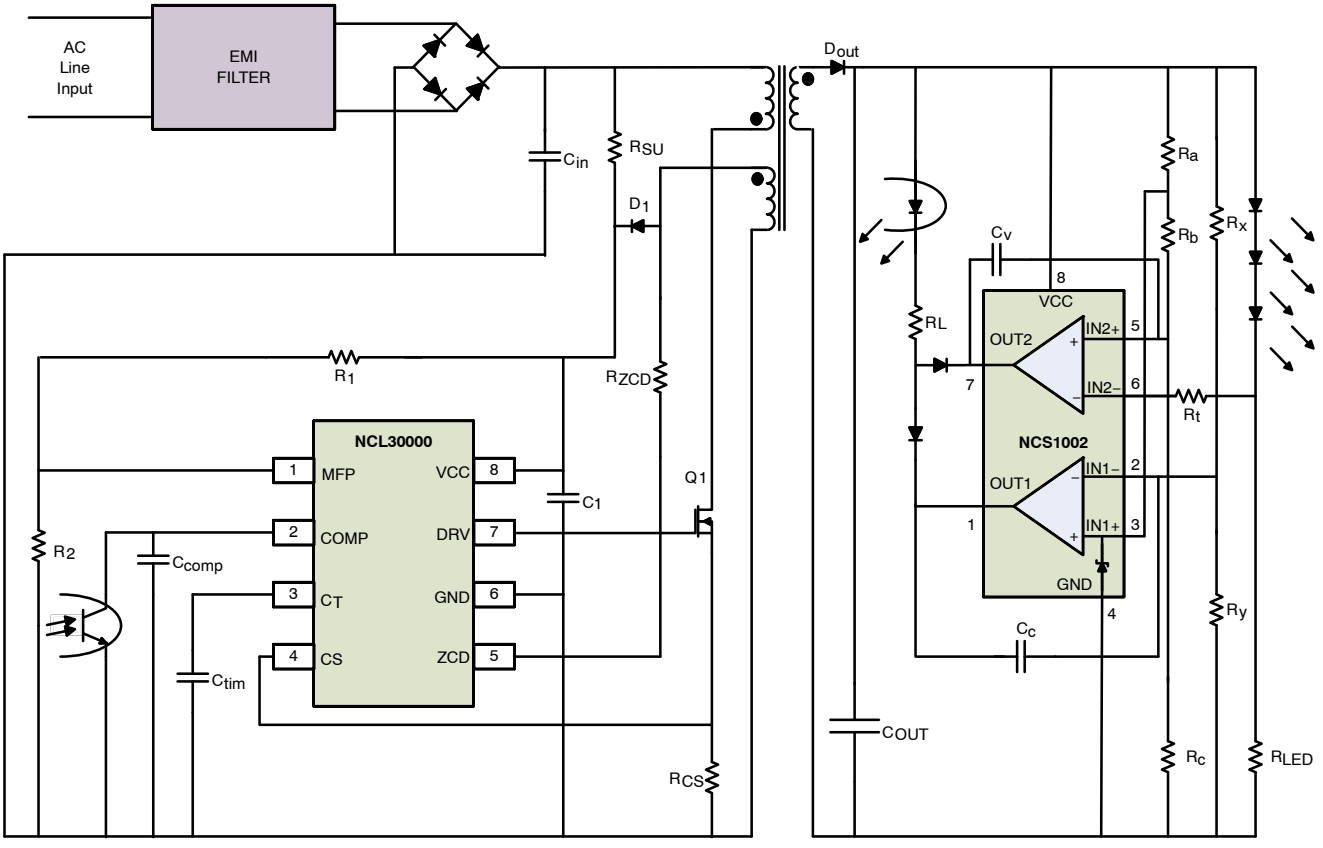

Figure 2. Simplified Flyback Application with Secondary side Constant Current Control

Overview

Figure 2 illustrates how the NCL30000 is configured to implement an isolated power factor corrected flyback switch mode power supply. On the secondary side is the NCS1002, a constant voltage, constant current controller which senses the average LED current and the output voltage and provides a feedback control signal to the primary side through an opto-coupler interface. One of the key benefits of active power factor correction is that it makes the load appear like a linear resistance similar to an incandescent bulb. High power factor requires generally sinusoidal line current and minimal phase displacement between the line current and voltage. The NCL30000 operates in a fixed on-time variable frequency mode where the power switch is on for the same length of time over a half cycle of input power. The current in the primary of the transformer starts at zero each switching cycle and is directly proportional to the applied voltage times the on-time. Therefore with a fixed on-time, the current will follow the applied voltage generating a current of the same shape. Just as in a traditional boost PFC circuit, the control bandwidth is low so that the on-time is constant throughout a single line cycle. The feedback signal from the secondary side is used to modify the average on-time so the current through the LEDs is properly regulated regardless of forward voltage variation of the LED string.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
MFP Voltage	V_{MFP}	−0.3 to 10	V
MFP Current	I_{MFP}	±10	mA
COMP Voltage	$V_{Control}$	−0.3 to 6.5	V
COMP Current	$I_{Control}$	−2 to 10	mA
Ct Voltage	V_{Ct}	−0.3 to 6	V
Ct Current	I_{Ct}	±10	mA
CS Voltage	V_{CS}	−0.3 to 6	V
CS Current	I_{CS}	±10	mA
ZCD Voltage	V_{ZCD}	−0.3 to 10	V
ZCD Current	I_{ZCD}	±10	mA
DRV Voltage	V_{DRV}	−0.3 to V_{CC}	V
DRV Sink Current	$I_{DRV(sink)}$	800	mA
DRV Source Current	$I_{DRV(source)}$	500	mA
Supply Voltage	V_{CC}	−0.3 to 20	V
Supply Current	I_{CC}	±20	mA
Power Dissipation (T_A = 70°C, 2.0 Oz Cu, 55 mm^2 Printed Circuit Copper Clad)	P_D	450	mW
Thermal Resistance Junction-to-Ambient (2.0 Oz Cu, 55 mm^2 Printed Circuit Copper Clad) Junction-to-Air, Low conductivity PCB (Note 3) Junction-to-Air, High conductivity PCB (Note 4)	 $R_{\theta JA}$ $R_{\theta JA}$	 178 168 127	°C/W
Operating Junction Temperature Range	T_J	−40 to 125	°C
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature (Soldering, 10 s)	T_L	300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1−8: Human Body Model 2000 V per JEDEC Standard JESD22−A114E.
   Machine Model Method 200 V per JEDEC Standard JESD22−A115−A.
2. This device contains Latch-up protection and exceeds ±100 mA per JEDEC Standard JESD78.
3. As mounted on a 40 × 40 × 1.5 mm FR4 substrate with a single layer of 80 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 low conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 40 × 40 × 1.5 mm FR4 substrate with a single layer of 650 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 high conductivity test PCB. Test conditions were under natural convection or zero air flow.

Table 3. ELECTRICAL CHARACTERISTICS
V_{MFP} = 2.4 V, $V_{Control}$ = 4 V, Ct = 1 nF, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{DRV} = 1 nF, V_{CC} = 12 V, unless otherwise specified
(For typical values, T_J = 25°C. For min/max values, T_J = −40°C to 125°C, unless otherwise specified)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Startup Voltage Threshold	V_{CC} Increasing	$V_{CC(on)}$	11	12	12.5	V
Minimum Operating Voltage	V_{CC} Decreasing	$V_{CC(off)}$	8.8	9.5	10.2	V
Supply Voltage Hysteresis		H_{UVLO}	2.2	2.5	2.8	V
Startup Current Consumption	0 V < V_{CC} < $V_{CC(on)}$ − 200 mV	$I_{cc(startup)}$	–	24	35	μA
No Load Switching Current Consumption	C_{DRV} = Open, 70 kHz Switching, V_{CS} = 2 V	I_{cc1}	–	1.4	1.7	mA
Switching Current Consumption	70 kHz Switching, V_{CS} = 2 V	I_{cc2}	–	2.1	2.6	mA
Fault Condition Current Consumption	No Switching, V_{MFP} = 0 V	$I_{cc(fault)}$	–	0.75	0.95	mA
OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
Overvoltage Detect Threshold	V_{MFP} = Increasing	V_{OVP}/V_{REF}	105	106	108	%
Overvoltage Hysteresis		$V_{OVP(HYS)}$	20	60	100	mV
Overvoltage Detect Threshold Propagation Delay	V_{MFP} = 2 V to 3 V ramp, dV/dt = 1 V/μs V_{MFP} = V_{OVP} to V_{DRV} = 10%	t_{OVP}	–	500	800	ns
Undervoltage Detect Threshold	V_{MFP} = Decreasing	V_{UVP}	0.25	0.31	0.4	V
Undervoltage Detect Threshold Propagation Delay	V_{MFP} = 1 V to 0 V ramp, dV/dt = 10 V/μs V_{MFP} = V_{UVP} to V_{DRV} = 10%	t_{UVP}	100	200	300	ns
ERROR AMPLIFIER						
Voltage Reference	T_J = 25°C T_J = −40°C to 125°C	V_{REF}	2.475 2.460	2.500 2.500	2.525 2.540	V
Voltage Reference Line Regulation	$V_{CC(on)}$ + 200 mV < V_{CC} < 20 V	$V_{REF(line)}$	−10	–	10	mV
Error Amplifier Current Capability	V_{MFP} = 2.6 V V_{MFP} = 1.08*V_{REF} V_{MFP} = 0.5 V	$I_{EA(sink)}$ $I_{EA(sink)OVP}$ $I_{EA(source)}$	6 10 −110	10 20 −210	20 30 −250	μA
Transconductance	V_{MFP} = 2.4 V to 2.6 V T_J = 25°C T_J = −40°C to 125°C	gm	 90 70	 110 110	 120 135	μS
Feedback Pin Internal Pull−Down Resistor	V_{MFP} = V_{UVP} to V_{REF}	R_{MFP}	2	4.6	10	MΩ
Feedback Bias Current	V_{MFP} = 2.5 V	I_{MFP}	0.25	0.54	1.25	μA
Control Bias Current	V_{MFP} = 0 V	$I_{Control}$	−1	–	1	μA
Maximum Control Voltage	$I_{Control(pullup)}$ = 10 μA, V_{MFP} = V_{REF}	V_{EAH}	5	5.5	6	V
Minimum Control Voltage to Generate Drive Pulses	$V_{Control}$ = Decreasing until V_{DRV} is low, V_{Ct} = 0 V	$Ct_{(offset)}$	0.37	0.65	0.88	V
Control Voltage Range	V_{EAH} − $Ct_{(offset)}$	$V_{EA(DIFF)}$	4.5	4.9	5.3	V

Table 3. ELECTRICAL CHARACTERISTICS (Continued)
V_{MFP} = 2.4 V, $V_{Control}$ = 4 V, Ct = 1 nF, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{DRV} = 1 nF, V_{CC} = 12 V, unless otherwise specified
(For typical values, T_J = 25°C. For min/max values, T_J = −40°C to 125°C, unless otherwise specified)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
RAMP CONTROL						
Ct Peak Voltage	V_{COMP} = open	$V_{Ct(MAX)}$	4.775	4.93	5.025	V
On Time Capacitor Charge Current	V_{COMP} = open V_{Ct} = 0 V to $V_{Ct(MAX)}$	I_{charge}	235	275	297	μA
Ct Capacitor Discharge Duration	V_{COMP} = open V_{Ct} = $V_{Ct(MAX)}$ −100 mV to 500 mV	$t_{Ct(discharge)}$	–	50	150	ns
PWM Propagation Delay	dV/dt = 30 V/μs V_{Ct} = $V_{Control}$ − $Ct_{(offset)}$ to V_{DRV} = 10%	t_{PWM}	–	130	220	ns
ZERO CURRENT DETECTION						
ZCD Arming Threshold	V_{ZCD} = Increasing	$V_{ZCD(ARM)}$	1.25	1.4	1.55	V
ZCD Triggering Threshold	V_{ZCD} = Decreasing	$V_{ZCD(TRIG)}$	0.6	0.7	0.83	V
ZCD Hysteresis		$V_{ZCD(HYS)}$	500	700	900	mV
ZCD Bias Current	V_{ZCD} = 5 V	I_{ZCD}	− 2	–	+ 2	μA
Positive Clamp Voltage	I_{ZCD} = 3 mA	$V_{CL(POS)}$	9.8	10	12	V
Negative Clamp Voltage	I_{ZCD} = −2 mA	$V_{CL(NEG)}$	−0.9	−0.7	−0.5	V
ZCD Propagation Delay	V_{ZCD} = 2 V to 0 V ramp, dV/dt = 20 V/μs V_{ZCD} = $V_{ZCD(TRIG)}$ to V_{DRV} = 90%	t_{ZCD}	–	100	170	ns
Minimum ZCD Pulse Width		t_{SYNC}	–	70	–	ns
Maximum Off Time in Absence of ZCD Transition	Falling V_{DRV} = 10% to Rising V_{DRV} = 90%	t_{start}	75	165	300	μs
DRIVE						
Drive Resistance	I_{source} = 100 mA I_{sink} = 100 mA	R_{OH} R_{OL}	– –	12 6	20 13	Ω
Rise Time	10% to 90%	t_{rise}	–	35	80	ns
Fall Time	90% to 10%	t_{fall}	–	25	70	ns
Drive Low Voltage	V_{CC} = $V_{CC(on)}$−200 mV, I_{sink} = 10 mA	$V_{out(start)}$	–	–	0.2	V
CURRENT SENSE						
Current Sense Voltage Threshold		V_{ILIM}	0.45	0.5	0.55	V
Leading Edge Blanking Duration	V_{CS} = 2 V, V_{DRV} = 90% to 10%	t_{LEB}	100	195	350	ns
Overcurrent Detection Propagation Delay	dV/dt = 10 V/μs V_{CS} = V_{ILIM} to V_{DRV} = 10%	t_{CS}	40	100	170	ns
Current Sense Bias Current	V_{CS} = 2 V	I_{CS}	−1	–	1	μA

TYPICAL CHARACTERISTICS

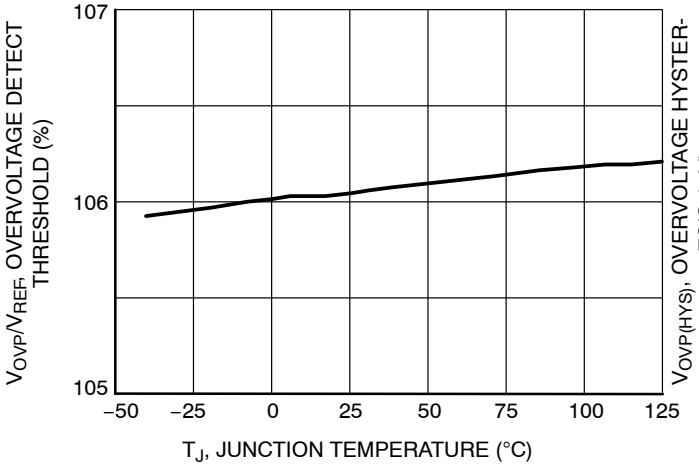

Figure 3. Overvoltage Detect Threshold vs. Junction Temperature

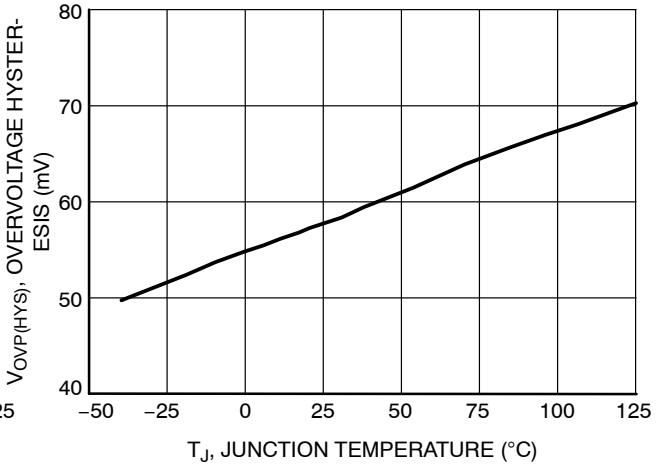

Figure 4. Overvoltage Hysteresis vs. Junction Temperature

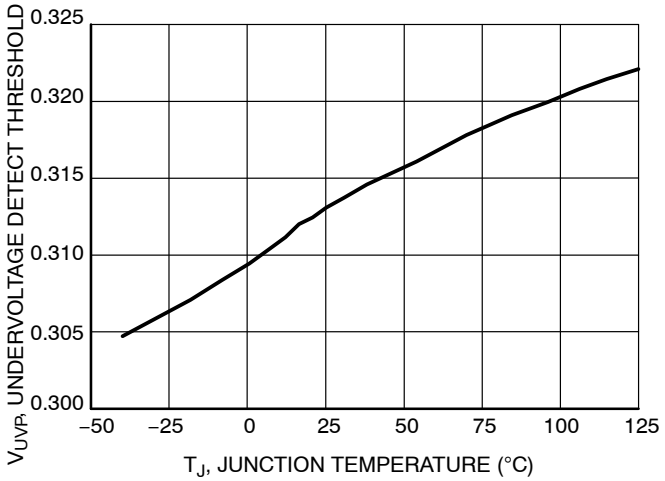

Figure 5. Undervoltage Detect Threshold vs. Junction Temperature

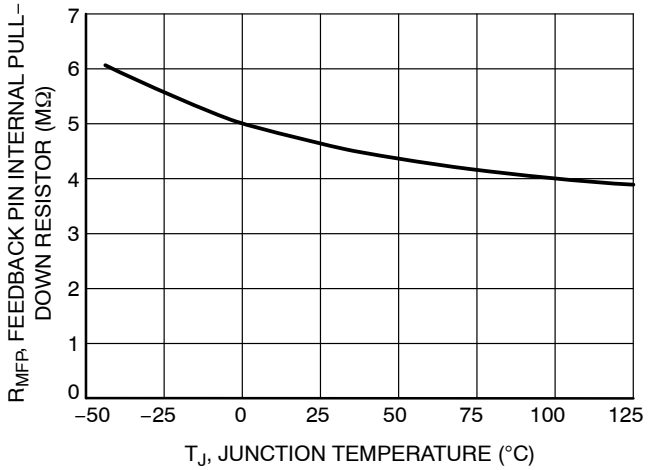

Figure 6. MFP Pin Internal Pull−Down Resistor vs. Junction Temperature

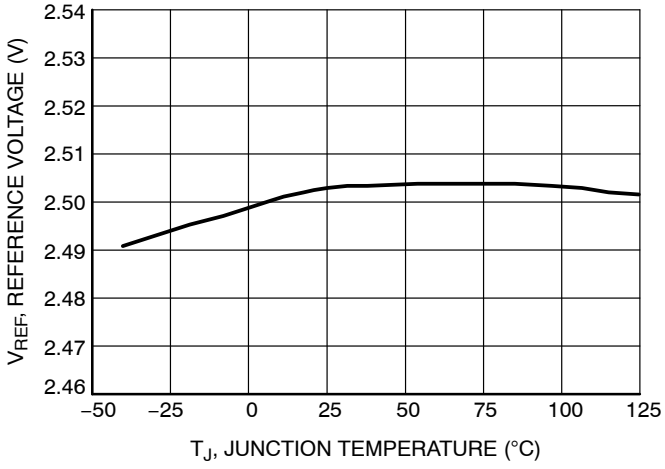

Figure 7. Reference Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS

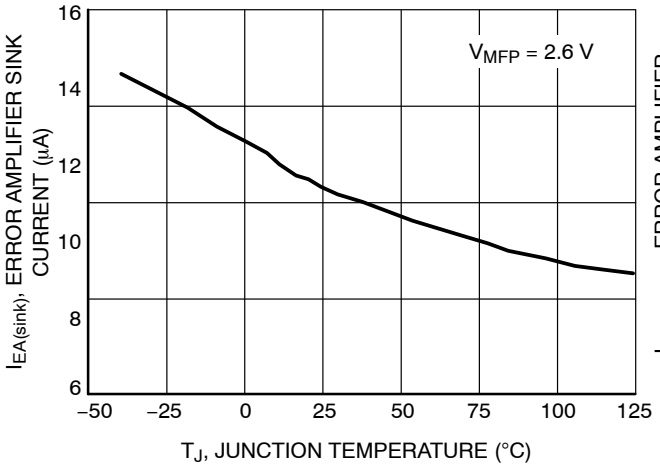

Figure 8. Error Amplifier Sink Current vs. Junction Temperature

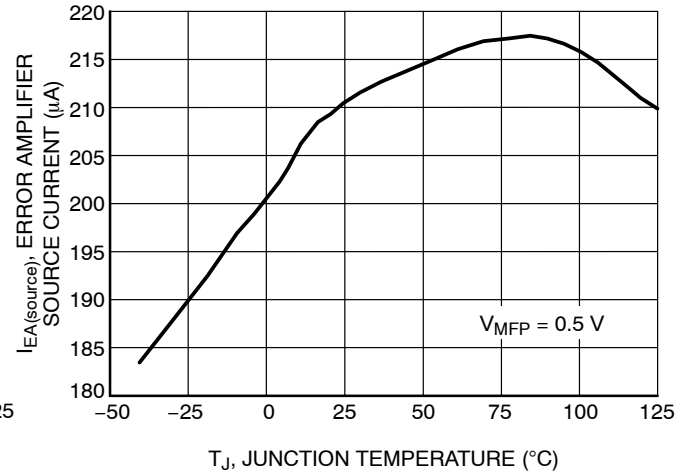

Figure 9. Error Amplifier Source Current vs. Junction Temperature

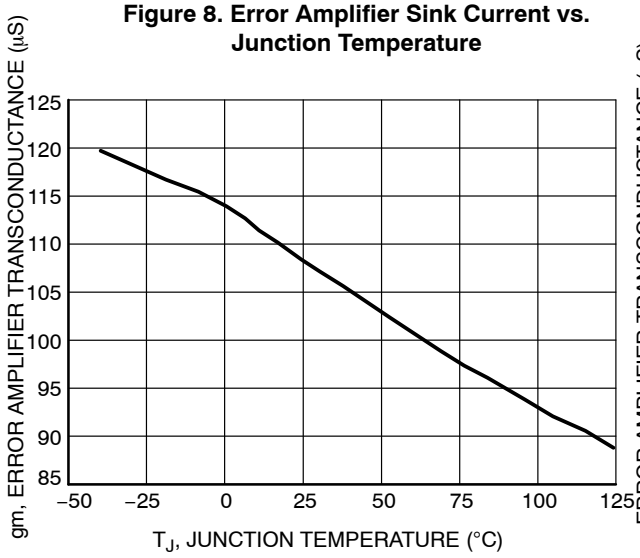

Figure 10. Error Amplifier Transconductance vs. Junction Temperature

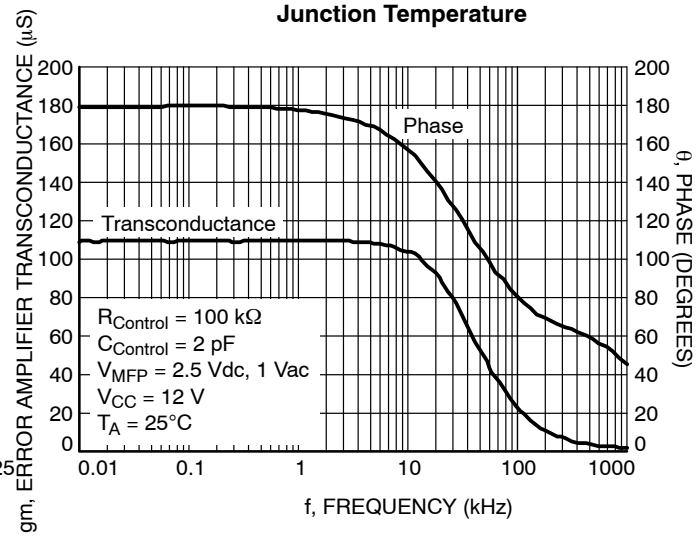

Figure 11. Error Amplifier Transconductance and Phase vs. Frequency

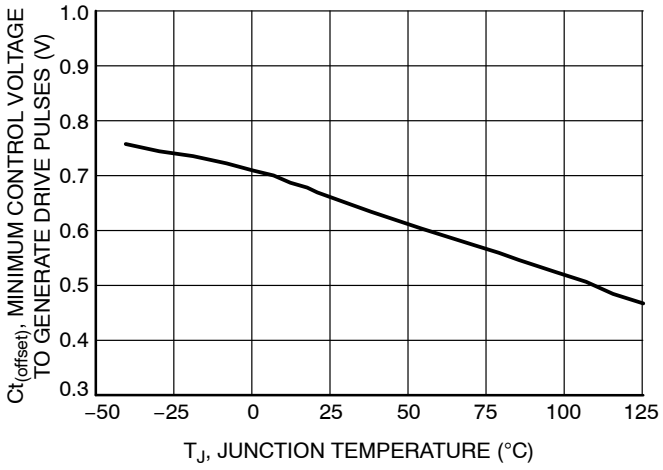

Figure 12. Minimum Control Voltage to Generate Drive Pulses vs. Junction Temperature

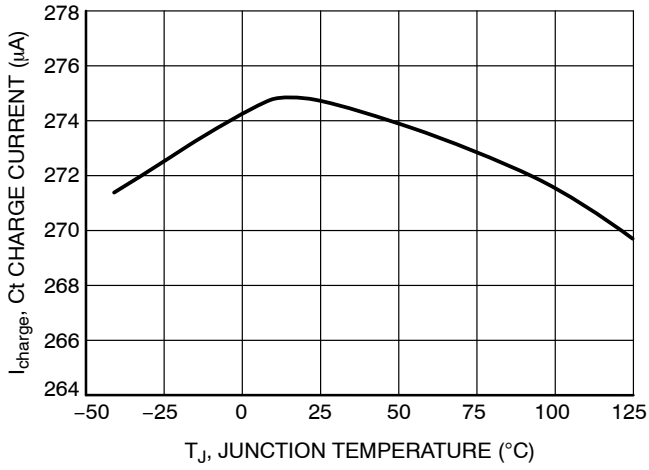

Figure 13. On Time Capacitor Charge Current vs. Junction Temperature

TYPICAL CHARACTERISTICS

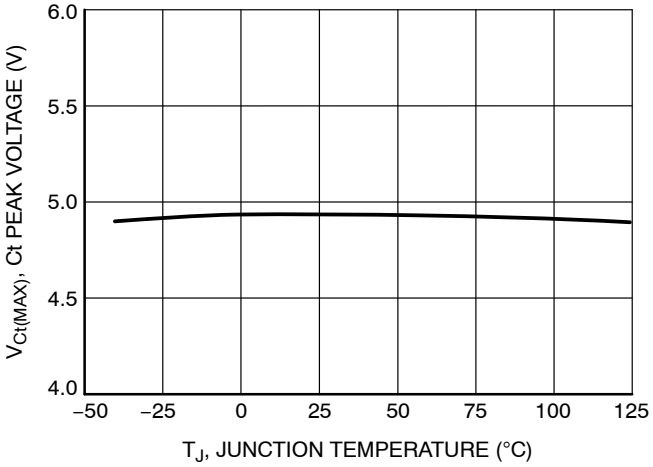

Figure 14. Ct Peak Voltage vs. Junction Temperature

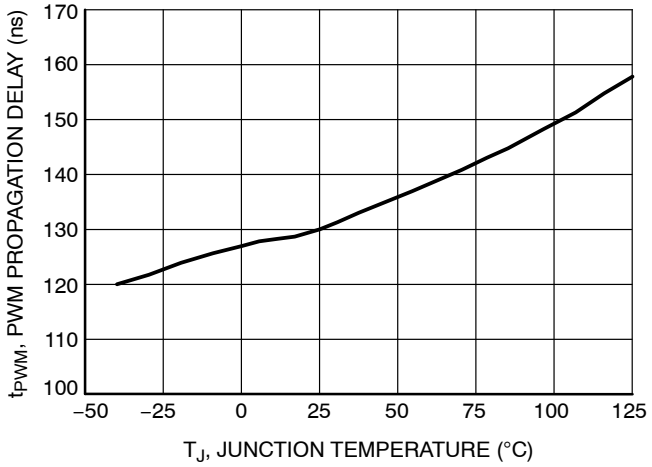

Figure 15. PWM Propagation Delay vs. Junction Temperature

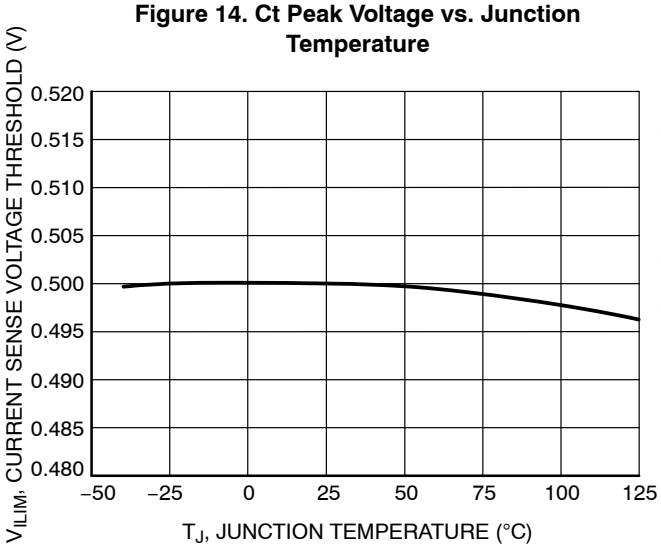

Figure 16. Current Sense Voltage Threshold vs. Junction Temperature

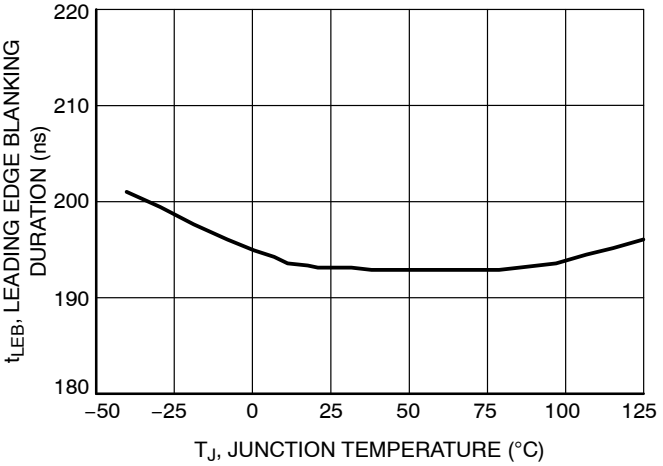

Figure 17. Leading Edge Blanking Duration vs. Junction Temperature

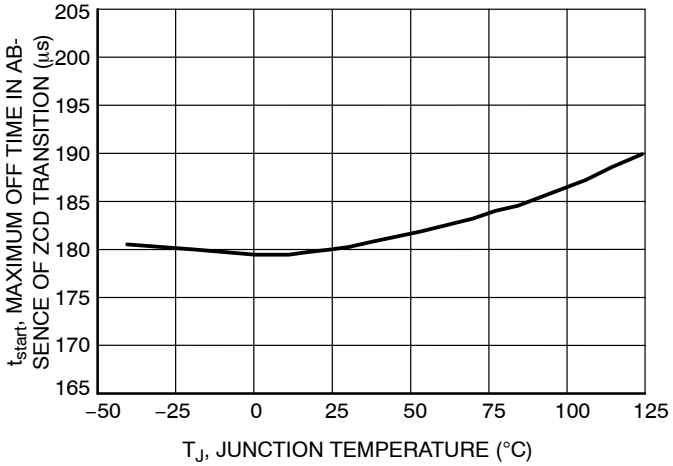

Figure 18. Maximum Off Time in Absence of ZCD Transition vs. Junction Temperature

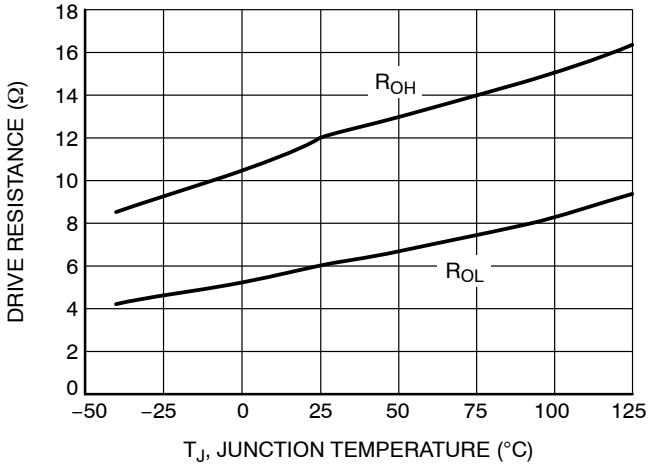

Figure 19. Drive Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS

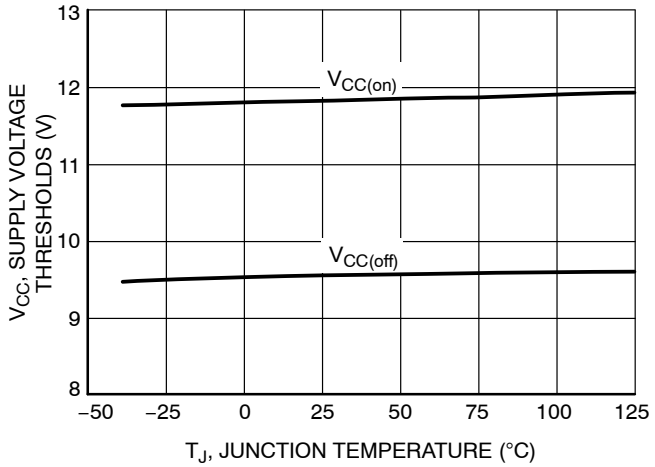

Figure 20. Supply Voltage Thresholds vs. Junction Temperature

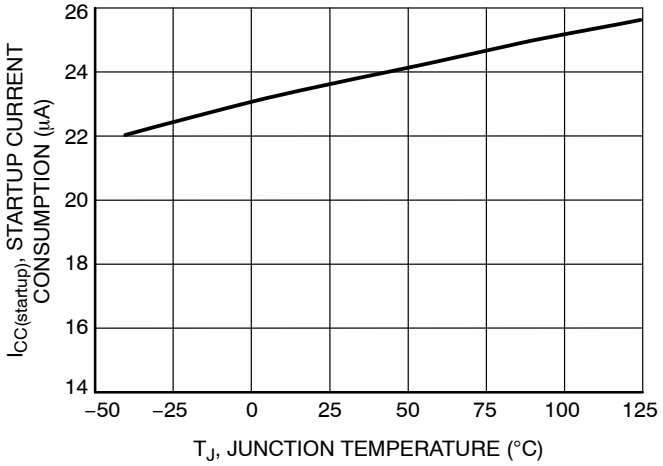

Figure 21. Startup Current Consumption vs. Junction Temperature

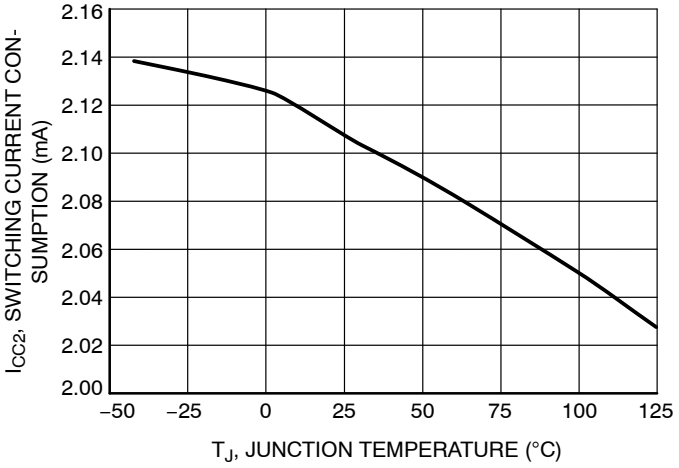

Figure 22. Switching Current Consumption vs. Junction Temperature

THEORY OF OPERATION

High power factor requires generally sinusoidal line current and minimal phase displacement between the line current and voltage. Normally this is not the case with a traditional isolated flyback topology so the first step to achieve high power factor is to have minimal capacitance before the switching stage to allow a more sinusoidal input current. A simplified block diagram is illustrated in Figure 23. Since the input bulk capacitor has virtually been eliminated except for a small capacitor, the voltage to the flyback converter now follows a rectified sine shape at twice the line frequency. By employing a critical conduction mode control technique such that the input current is kept to the same shape, high power factor can be achieved. The NCL30000 is a voltage mode, fixed on-time controller specifically intended for such applications.

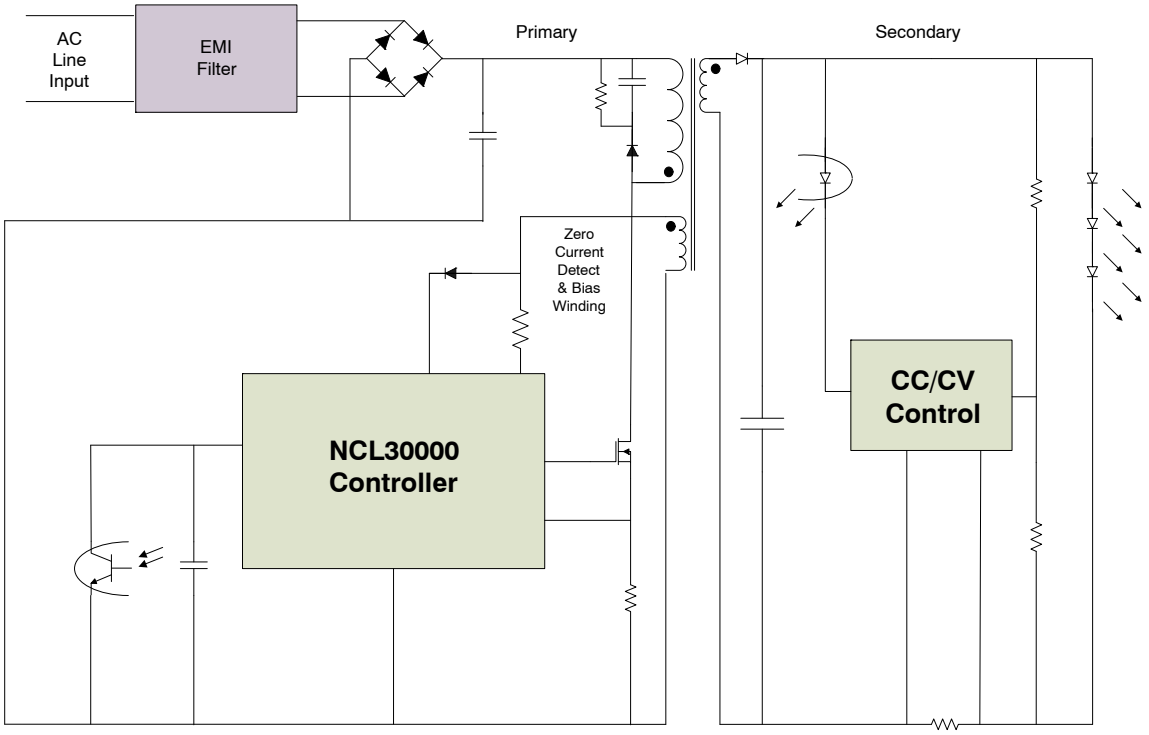

Figure 23. Simplified Block Diagram

Since the input voltage waveform to the flyback is sinusoidal, with a fixed on-time control scheme, the current through the transformer primary will increase directly with the line voltage and the average current drawn from the line will have a sinusoidal shape. When the switch is turned off the energy from the primary will be transferred to the secondary. By monitoring the auxiliary winding the controller can detect when the secondary current reaches zero and restart the switching cycle to transfer additional energy to the load. The current in the primary of the transformer starts at zero each switching cycle and is directly proportional to the applied voltage times the on-time. One of the primary benefits of this CrM approach is that we can operate with zero current switching which results in a very efficient architecture for low to medium power applications.

A secondary side control loop monitors the average LED current and adjusts the on-time to maintain proper regulation. To achieve high power factor, the control loop bandwidth must be sufficiently low such that the on-time is constant across a line half cycle. Since the off time varies depending on the energy transferred through the transformer and the load, the switching frequency varies with load and line. Figure 24 illustrates the theoretical current waveform through the primary and secondary transformer windings. The energy delivered to the load through the transformer will follow the product of voltage and current which is a sine-squared shape. As a result of this sine-squared energy transfer, the load will experience ripple at twice the line frequency, either 100 or 120 Hz depending on the source. The delivered power through the transformer starts at zero, rises to a peak and returns to zero following the shape of the rectified input line. The 100/120 Hz ripple is superimposed on the normal switching waveform of the PWM converter. The maximum on-time must be set such that the maximum power is delivered at the minimum required operation voltage. The LED current required for a particular application is generally specified as an average value. LEDs can tolerate ripple current as long as the ripple frequency is above the visible range of the human eye and the peak current does not exceed the rating of the LEDs. Just like a standard flyback, the output capacitors filter the pulsing power from the transformer to match the average current required by the LED and must be sized appropriately to limit the peak current through the LEDs.

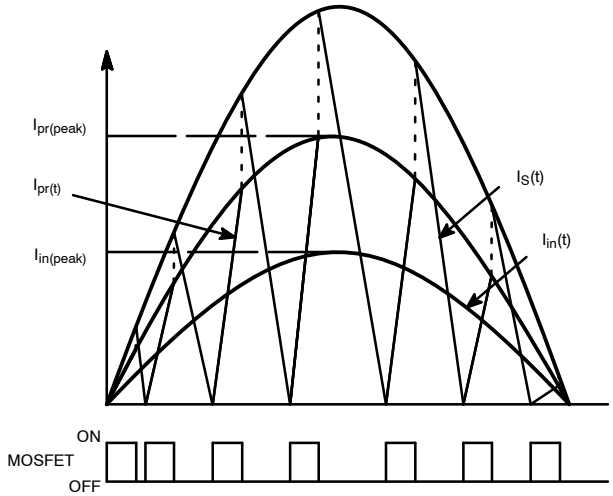

Figure 24. Theoretical Switching Waveform

The LED current is compared to a reference and an error signal is passed to the NCL30000 controller to maintain the desired average level. This error signal adjusts the on-time of the power switch to pass the required energy through the flyback transformer to achieve proper regulation of the LED load. Just like in a traditional PFC boost converter, the loop bandwidth must be low enough to filter out the twice line frequency ripple otherwise the power factor correction element of the circuit will be compromised. In the event of an open LED fault, a constant voltage loop regulates the output voltage across the output capacitor to assure safe operation.

The NCL30000 (refer to the block diagram – Figure 1) is composed of 4 key functional blocks along with protection circuitry to ensure reliable operation of the controller.

- On-time Control
- Zero Current Detection Control
- MOSFET Gate Driver
- Startup and V_{CC} Management

On Time Control

The on-time control circuitry (Figure 25) consists of a precision current source which charges up an external capacitor (C_t) in a linear ramp. The voltage on C_t (after removing an internal offset) is compared to an external control voltage and the output of the comparator is used to turn off the output driver thus terminating the switching cycle. A signal from the driver is fed back to the on-time control block to discharge the C_t capacitor thus preparing the circuit for the start of the next switching cycle.

The state of $V_{control}$ is determined by the external regulation loop and varies with the rms input voltage and the output load. To achieve high power factor, the regulation loop is designed so that in steady state, the $V_{control}$ value is held constant over a line half cycle. This results in fixed on time operation. The range of on-time is determined by the charging slope of the C_t capacitor and is clamped at 4.93 V nominal. The C_t capacitor is sized to ensure that the required on-time is reached at maximum output power and the minimum input line voltage condition. Because the ramp has a wide dynamic range, the control loop can accommodate wide variation of line voltage and load power range.

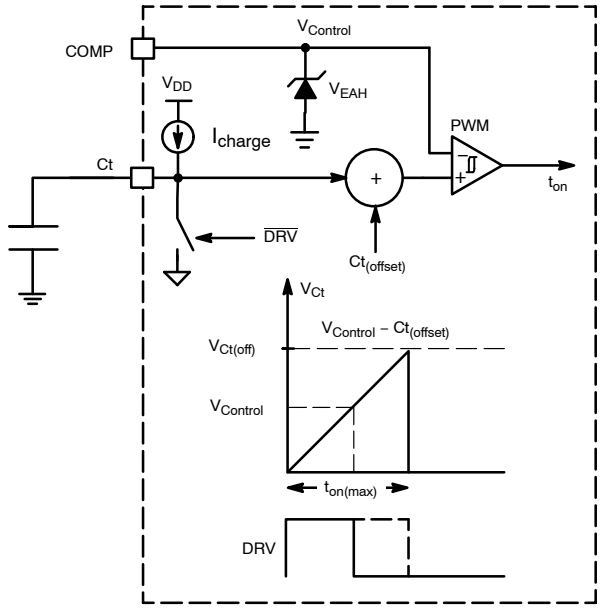

Figure 25. On Time Control

Off Time Sequence

In a fixed on-time CRM flyback converter, energy stored in the primary of the flyback transformer varies directly with input line voltage on a cycle-by-cycle basis. When the switching cycle is terminated, the energy stored in the transformer is transferred to the secondary. The auxiliary winding used to provide bias to the NCL30000 is also used to detect when the current in the secondary winding has dropped to zero. This is illustrated in Figure 26.

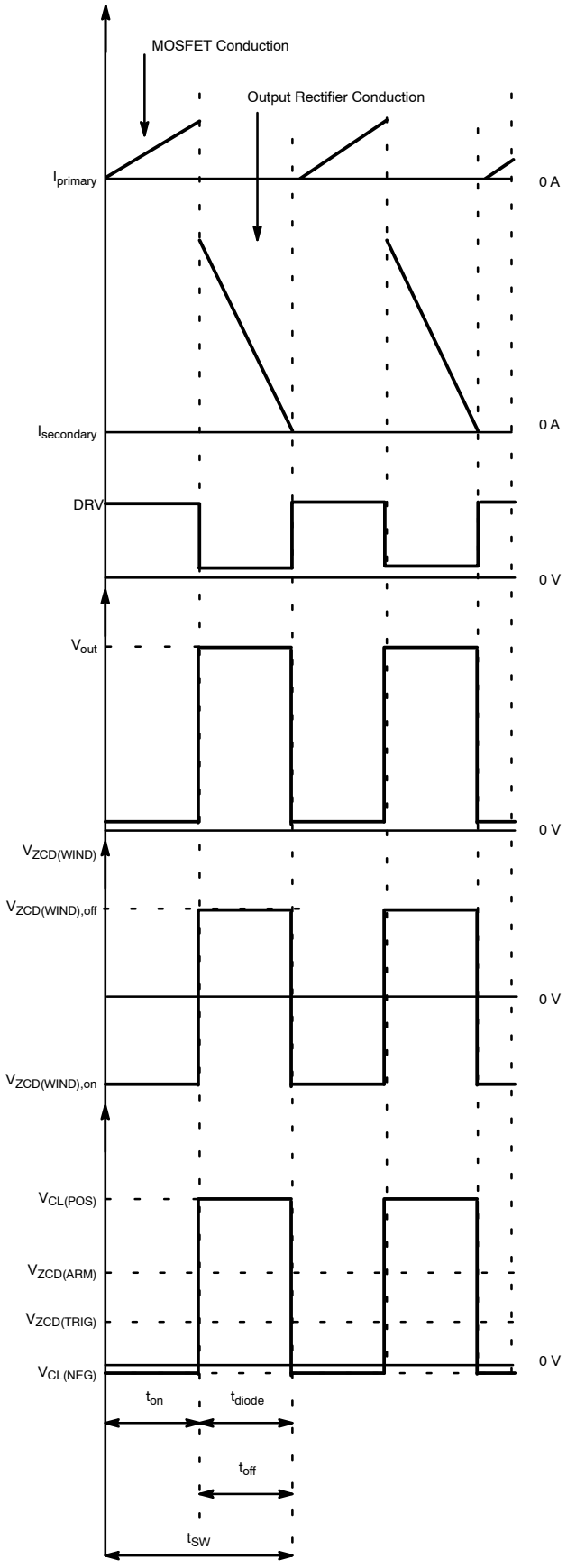

Figure 26. Ideal CrM Waveforms with ZCD Winding

ZCD Detection Block

A dedicated circuit block is necessary to implement the zero current detection**.** The NCL30000 provides a separate input pin to signal the controller to turn the power switch back on just after the flyback transformer discharges all the stored energy to the secondary winding. When the output winding current reaches zero the winding voltage will reverse. Since all windings of the transformer reflect the same voltage characteristic this voltage reversal appears on the primary bias winding. Coupling the winding voltage to the ZCD input of the NCL30000 allows the controller to start the next switching cycle at the precise time. To avoid inadvertent false triggering, the ZCD input has a dual comparator input structure to arm the latch when the ZCD detect voltage rises above 1.4 V (nominal) thus setting the latch. When the voltage on ZCD falls below 0.7 V (nominal) a zero current event is detected and a signal is asserted which initiates the next switching cycle. This is illustrated in Figure 27. The input of the ZCD has an internal circuit which clamps the positive and negative voltage excursions on this pin. The current into or out of the ZCD pin must be limited to ±10 mA with an external resistor.

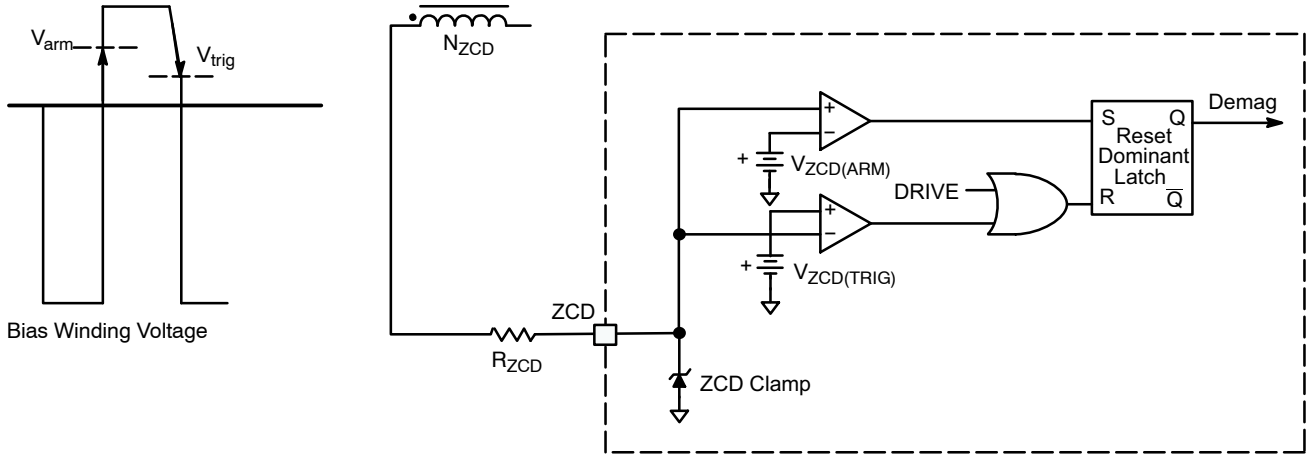

Figure 27. ZCD Operation

At startup, there is no energy in the ZCD winding and no voltage signal to activate the ZCD comparators. To enable the controller to start under these conditions, an internal watchdog timer is provided which initiates a switching cycle in the event that the output drive has been off for more than 180 μs (nominal).

The timer is deactivated only under an OVP or UVP fault condition which will be discussed in the next section.

Overcurrent Protection (OCP)

The dedicated CS pin of the NCL30000 senses the current through the MOSFET switch and the primary side of the transformer. This provides an additional level of protection in the event of a fault. If the voltage of the CS pin exceeds V_{ILIM}, the internal comparator will detect the event and turn off the MOSFET. The peak switch current is calculated using Equation 1:

$$I_{SW(peak)} = \frac{V_{ILIM}}{R_{sense}} \qquad \text{(eq. 1)}$$

To avoid the probability of false switching, the NCL30000 incorporated a built in leading edge blanking circuit (LEB) which masks the CS signal for a nominal time of 190 ns. If required, an optional RC filter can be added between R_{sense} and CS to provide additional filtering. This is illustrated below.

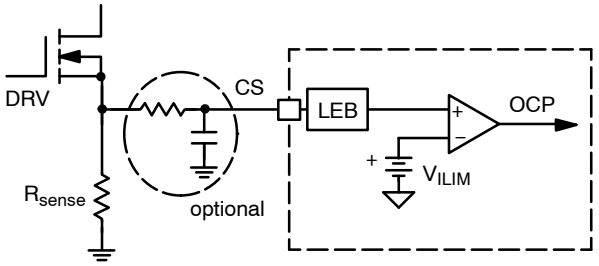

Figure 28. OCP Circuitry with Optional External RC Filter

MFP Input

The multi-function pin is connected to the input of the transconductance amplifier, the undervoltage and overvoltage protection comparators. This allows this pin to perform several functions. To place the device in standby, the MFP pin should be pulled below the V_{uvp} threshold. This is illustrated in Figure 29. Additionally, raising the MFP pin above V_{ovp} will also suspend switching activity but not place the controller in the standby mode. This can be used implement overvoltage monitoring on the bias winding and add an additional layer of fault protection.

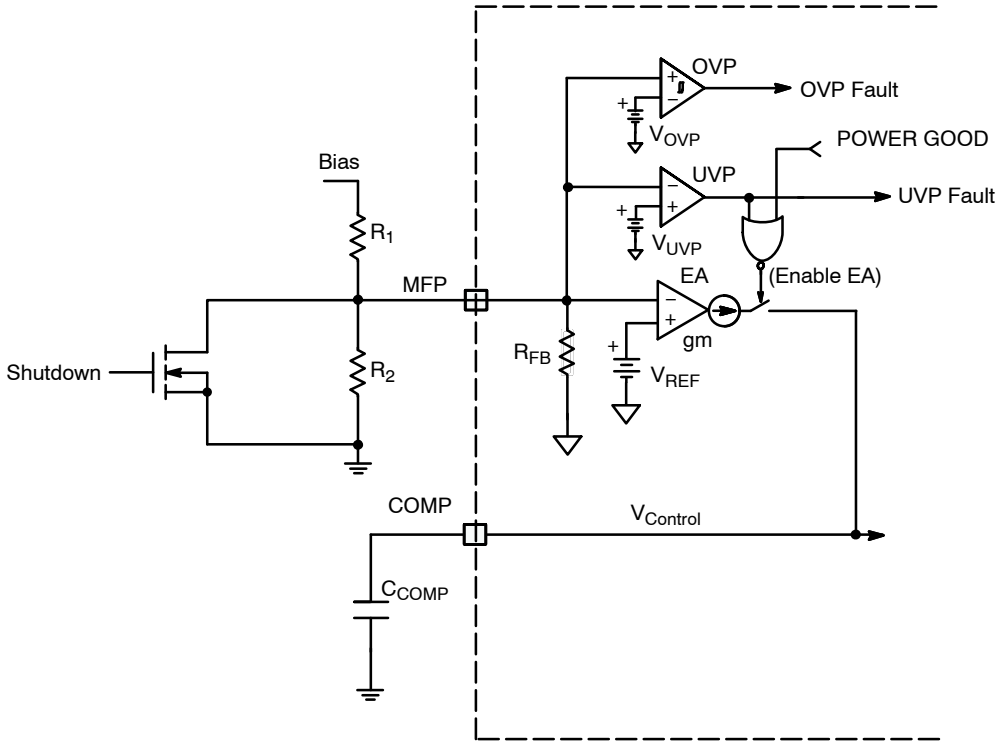

Figure 29. Multi−Function Pin Operation

The positive input of the transconductance amplifier is connected to a 2.5 V (nominal) reference. This allows the controller to be used in non-isolated applications where the MFP could be configured in a more classical feedback input configuration.

V_{CC} Management

The NCL30000 incorporates a supervisory circuitry to manage the startup and shutdown of the circuit. By managing the startup and keeping the initial startup current at less than 35 μA, a startup resistor connected between the rectified ac line and V_{CC} charges the V_{CC} capacitor to $V_{CC(on)}$. Turn on of the device occurs when the startup voltage has exceeded 12 V (nominal) when the internal reference and switching logic are enabled. A UVLO comparator with a hysteresis of 2.5 V nominal gives ample time for the device to start switching and allow the bias from the auxiliary winding to supply V_{CC}.

Example Design

A practical design case will be used to illustrate the overall power supply functional blocks and the overall design methodology. The power supply specification in this example is listed below and covers an extended universal input range which includes the normal 90−265 Vac for global power supplies with an extended upper range to support 277 Vac commercial lighting in the United States.

- Input voltage: 90 to 305 Vac
- Power factor: > 0.9
- Output current: 350 mA Typical
- LED load voltage: 12 to 50 Vdc
- Full Load Efficiency: > 85%

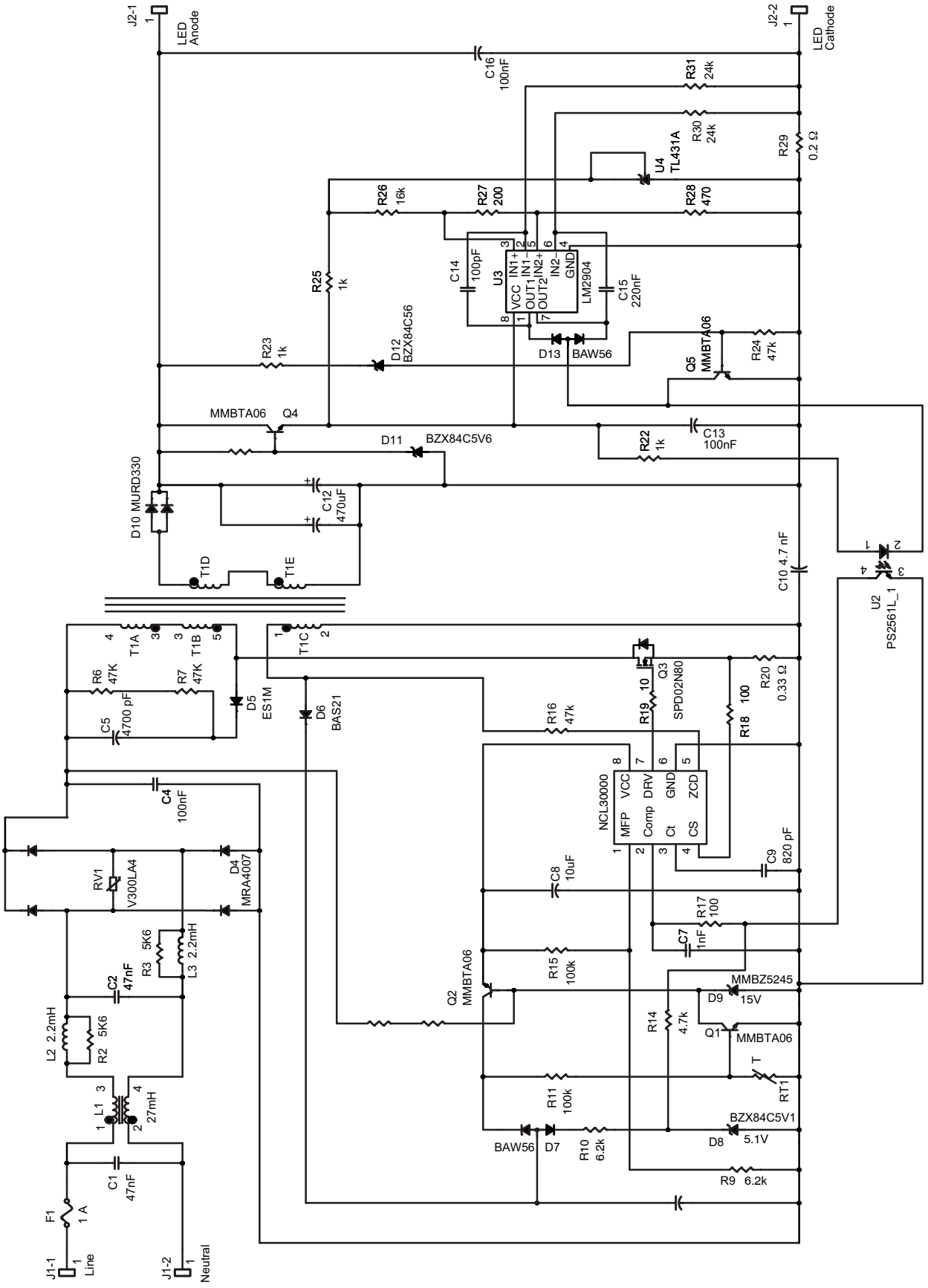

Figure 30. Wide Input Main, 4−15 LED 350 mA Load Schematic

Zero Current Detection (ZCD)

The signal controlling the ZCD function is taken from the primary bias winding. Raising the ZCD pin above 1.4 V arms the zero detection circuit. When the pin voltage subsequently falls below 0.7 V, the controller issues the command to turn the power switch back on. The current in or out of the ZCD pin must be limited to ±10 mA by an external resistor. For this reference circuit a resistance of 47 kΩ provides the required voltage thresholds and limits current to less than 10 mA.

Feedback Control

The secondary feedback signal is routed through an optocoupler to the primary side NCL30000 controller. LED current is measured with a 0.2 Ω resistor which for 350 mA has a voltage drop of 70 mV.

The control loop must be designed to filter out the rectified sine wave ripple component to provide an average feedback level to the pulse width controller. In order to maintain high power factor operation, the compensation components around the error amplifier must be set well below 50/60 Hz. The corner frequency typically falls between 10 and 40 Hz. The low frequency response means the control loop will be slow to compensate for rapidly changing situations. In particular, the slow response can introduce overshoot at turn on.

To compensate for the slow steady state loop this circuit utilizes a second current control loop to minimize overshoot. The second loop is set for higher than nominal operating current with a very fast response loop. This error amp takes control of the feedback loop until the main error amp is able to respond. In this way the maximum current is limited to safe established level.

The current set point of the fast control loop should be set above the peak of the ripple current of normal operation. U4 is a 2.5 V reference which in conjunction with R26, R27, and R28 establishes the nominal reference voltage of 70 mV mentioned above but also the higher threshold for the fast current loop. In this example, the average output current is 350 mA and the fast loop is set for a 500 mA level.

EMI Filter

The EMI filter attenuates the switching current drawn by the power converter reducing the high frequency harmonics to within conducted emissions limits. The filter must not degrade the power factor by introducing a phase shift of the current with the line-to-line or X capacitors. Low total capacitance will minimize this effect. Balancing these attributes is a performance tradeoff considering the wide input voltage requirements.

A multi-stage filter consisting of 27 mH common mode inductor and two 2.2 mH differential inductors working with two 47 nF capacitors provides sufficient attenuation to pass conducted emissions requirements. A 4.7 nF “Y1” capacitor bypasses common mode currents created by the power transformer.

The low input capacitance approach taken in this design to meet high power factor has the added benefit of not needing inrush current limiting.

Start-up Circuit and Primary Bias

Rapid start up is enhanced by the low current draw of the NCL30000. Resistors connected from the rectified ac line to the V_{CC} circuit provide start up power. Some of the current is needed for the control chip and bias network while the remaining portion charges up a storage capacitor. When the voltage on the capacitor reaches 12 V nominal, the internal references and logic of the NCL30000 are turned on and the part starts switching. The turn on comparator has hysteresis (2.5 V nominal) to ensure sufficient time for the auxiliary winding to start supplying current directly to the V_{CC} capacitor. Resistor divider R9 (6.2 kΩ) and R15 (100 kΩ) bias the MFP at the proper voltage to enable the NCL30000.

An optional thermal shutdown is implemented with positive temperature coefficient (PTC) thermistor RT1. This thermistor is placed close to the switching FET Q3 sensing temperature stress related to load and surrounding temperature. Situations causing excessive temperature will cause RT1 to switch to a high impedance turning off the NCL30000. When RT1 cools down, normal operation will resume.

Transformer Design

Single stage high power factor flyback converters process power in a sine-squared manner. To support the average LED load current, the flyback converter must be capable of processing 2 times the average output power. In this case, the flyback transformer is designed to handle a peak power of 42 W to power a 17.5 W LED load scaled for the efficiency. The complete details of the transformer design process are found in Application Note AND8451.

The NCL30000 is a variable frequency CrM controller and as such the transformer determines the operating frequency for a given set of input and output conditions. The transformer turns ratio is controlled by maximum input and output voltage and the ratings of the FET and output rectifier. In this case, the turns ratio from primary to secondary is set at 3.83.

Power switch on-time is set at the low line condition of 90 Vac or 126 V peak and maximum power of 17.5 W. On-time will be 13.3 μs maximum. Primary inductance is calculated from the minimum switching frequency and the conditions listed above as 1.57 mH.

Peak primary current of 1.11 A is calculated from the primary inductance, applied voltage, and on-time. Core flux density occurs at the peak of the input rectified sine wave. Primary turns are established from inductance, current, maximum flux density and core geometry as 92 turns. Primary turns, current, and maximum flux density set gap size and is approximately 0.016 inches for this transformer.

The primary 92 turns divided by the previously calculated ratio of 3.83 establishes secondary turns at 24. #26 triple

insulated wire is selected for compliance with safety agency isolation requirements.

The primary bias winding must supply 10.2 V to maintain NCL30000 operation. The minimum secondary voltage is 12 V and with 24 turns this means the bias winding needs 20.4 turns. Select 22 turns to meet the minimum.

For maximum primary to secondary coupling, the primary winding will be split in two equal sections with the secondary winding placed in between. The bias winding is wound on top of the second half of the primary winding.

FET Switch

The NCL30000 controller drives an external power FET controlling the current in the flyback transformer primary. The demonstration board was designed to accept the surface mount DPAK or through-hole TO−220 power packages. The 17.5 W target application in 50°C ambient works well with a DPAK package. The 800 V 2 A rated SPD02N80C3 was chosen.

Maximum primary current was calculated as 1.11 A. The NCL30000 has a 0.5 V over-current protection threshold. To allow for 25% margin, a minimum sense resistor of 0.348 Ω is required. A standard 0.33 Ω resistor will be selected. The current sense resistor is placed in the source lead of the power FET and coupled to the controller with a 100 Ω resistor. This resistance in conjunction with the inherent capacitance of the pin filters high frequency noise. In addition, a leading edge blanking (LEB) function is included in the controller. This feature avoids spurious activation of the over-current protection when the power FET is first turned on.

On-time Capacitor

Maximum FET switch on-time is controlled by the C_t capacitor. Limiting the maximum on-time reduces component stress in transient situations. The formula below establishes the capacitor value based on charging current of 297 μA and maximum voltage threshold of 4.775. The symbol η' represents the effective efficiency of the power transformer stage and secondary losses. It will always be greater than the measured wall plug efficiency which includes losses in the EMI filter and primary side compents.

$$C_t \approx \frac{\left(4 \cdot L_{pri} \cdot P_{out} \cdot I_{charge}\right)}{\left(\eta' \cdot V_{pk}{}^2 \cdot V_{CT(max)}\right)} \cdot \left(\frac{V_{pk}}{N \cdot V_{out}} + 1\right) \qquad \text{(eq. 2)}$$

$$C_t \approx \frac{\left(4 \cdot 0.00157 \cdot 17.5 \cdot 297\ \mu A\right)}{\left(0.95 \cdot \left(\sqrt{2} \cdot 90\right)^2 \cdot 4.775\ V\right)} \cdot \left(\frac{\sqrt{2} \cdot 90}{3.83 \cdot 50} + 1\right)$$

$$C_t \approx 740\ pF$$

The C_t equation is an approximation for simplification. For example, V_{pk} assumes no losses through the diode rectifier bridge and EMI filter. This establishes an initial starting point for the C_t capacitor and further optimization may be needed. For this design, 820 pF was used as the final value.

Output Filter

As previously discussed, a high power factor isolated single-stage converter processes power in a sine squared manner at twice the line frequency. Energy storage must be provided on the isolated secondary output just as in normal flyback converters however significantly more storage capacity is required due to the sine squared energy transfer characteristic. Capacitors are used to store energy as the peak of the 100 or 120 Hz rectified sine wave delivers maximum power and then releases the stored energy to the load when the rectified sine wave falls below the target output power. As the storage capacitor charges and discharges some ripple current is developed in the LED load. The magnitude of ripple voltage is controlled by the amount of filter capacitance and the impedance of the LED string. In this 350 mA application, two 470 μF capacitors are sufficient to provide 30% ripple.

High grade electrolytic capacitors should be selected to match driver lifetime with that of the LEDs. Higher temperature rated capacitors enhance lifetime for an optimal solution. To meet ripple requirements in single stage converters filter capacitance is generally high enough that capacitor ripple current is well below device ratings.

Secondary Bias

The average mode feedback compensation is intentionally set to a low frequency as described in the feedback section. The relatively large feedback compensation capacitor must charge to normal operating voltage after initial power up which introduces significant delay in regulation. Minimizing the required voltage change on the compensation capacitor allows the feedback loop to take control of the output quicker therefore reducing over-current conditions. Maintaining a low bias voltage reduces the required change in compensation capacitor voltage. For this example, a bipolar transistor and 5.6 V zener diode are employed to provide bias voltage of about 5 V. This bias transistor minimizes power loss and allows the LED driver to operate over a very wide range of output voltage. This circuit will support as few as 4 LEDs and up to 15 LEDs.

The secondary bias can be optimized if the application uses a specific number of LEDs. Fewer components and better efficiency can be realized by limiting the output voltage range and adding a secondary bias winding to the transformer.

Open Load Protection

The LED driver behaves like a current source where the output voltage is determined by the forward voltage of the LED string. As such, some protection is required to prevent damage in the event of an open LED situation. Transistor (Q5) and zener diode (D12) affords the necessary protection. A 56 V zener is used in this design example.

Performance Data for 90 to 305 Vac LED Driver

Shown below in Figure 31 is the line regulation and efficiency with a 36.9 V, 12 LED load. Note the output current does not vary much over the entire input voltage range. The data is based on the use of an EFD25 transformer.

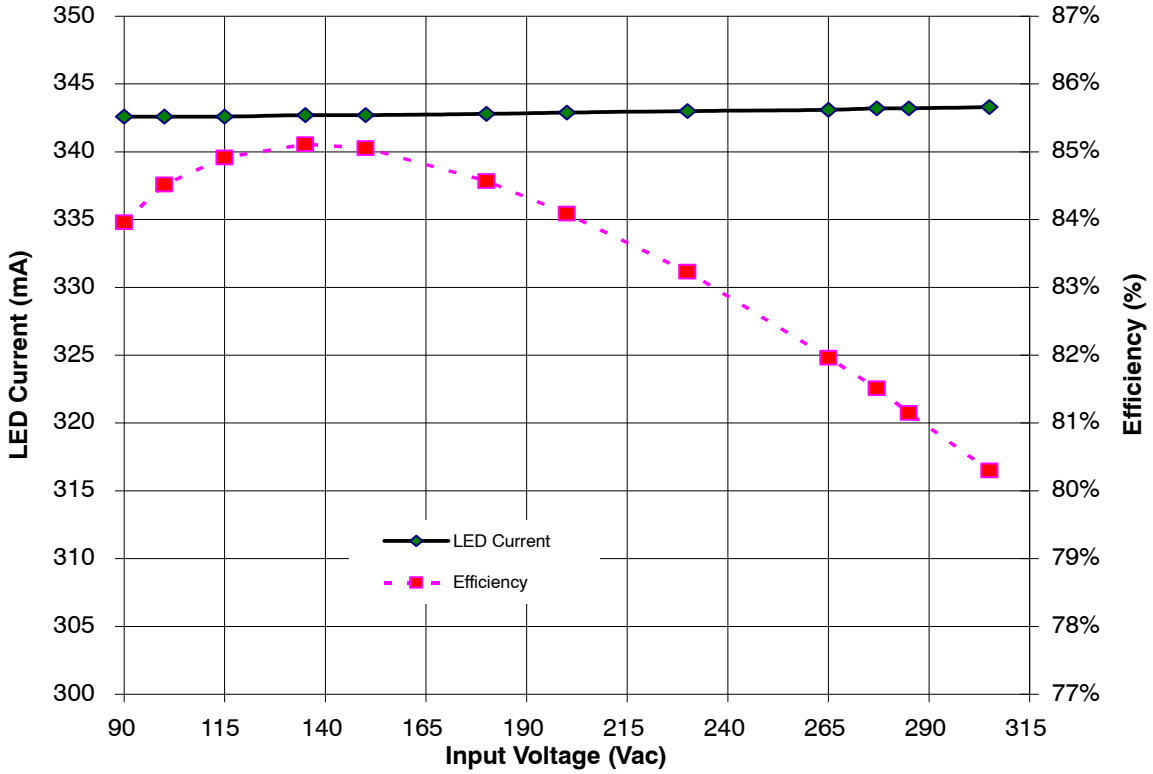

Figure 31. Output Current and Efficiency with 36.9 V Load

Power factor and Total Harmonic Distortion are shown in Figure 32 below.

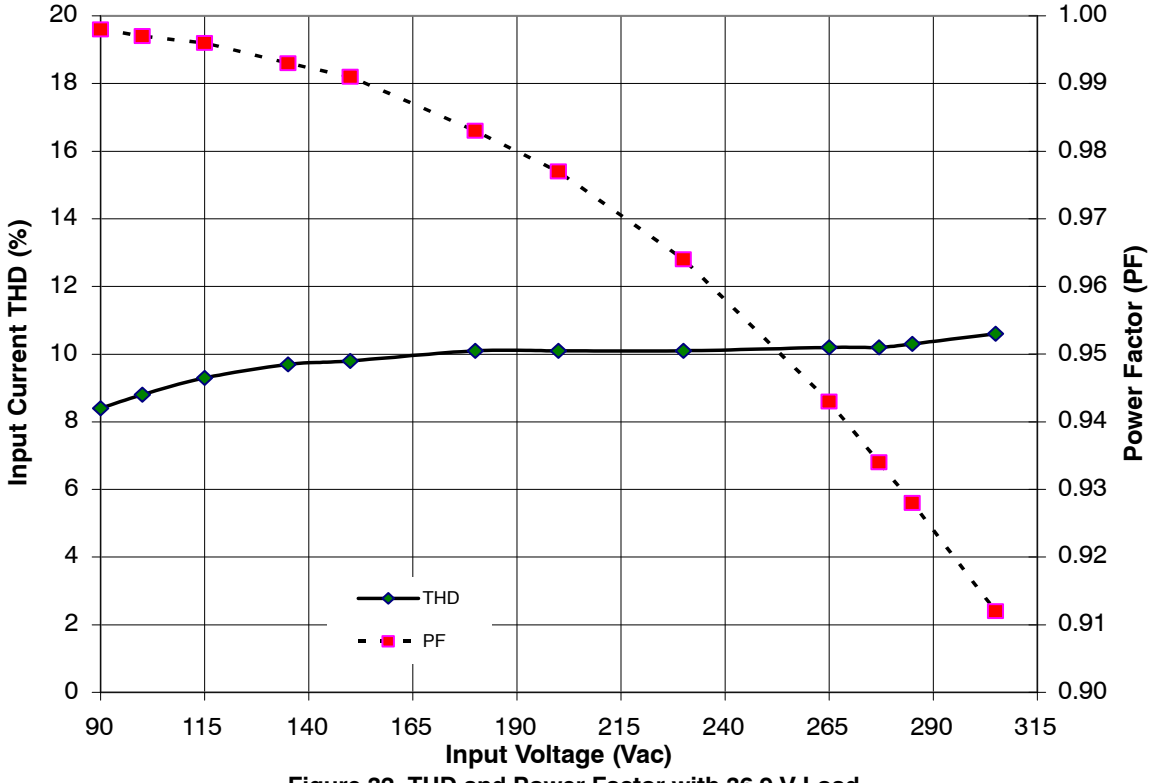

Figure 32. THD and Power Factor with 36.9 V Load

Load regulation from 12.3 to 52.5 (4 to 15 LEDs) for 115 and 230 Vac input is shown below in Figure 4. Efficiency for this range is also shown. Note the tight regulation. Efficiency is affected by the startup circuit losses in proportion to load and influenced by higher line voltage.

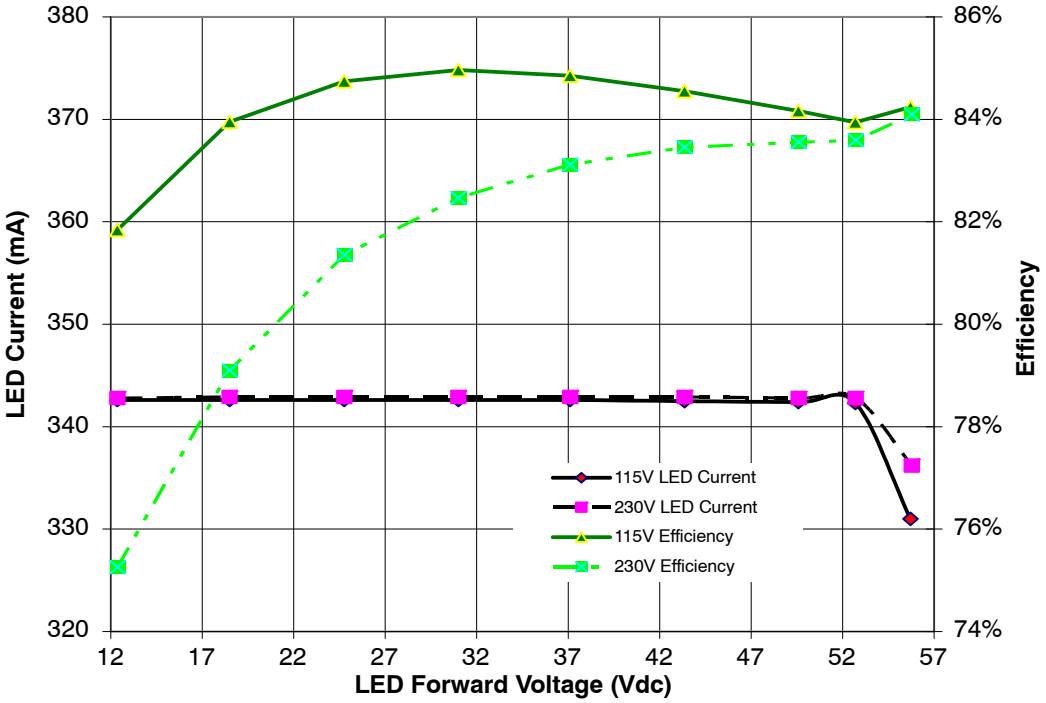

Figure 33. LED Current and Efficiency at 115 and 230 Vac

Figure 34 shows the current regulation as a function of output voltage (LED forward voltage). The control loop has been designed to support 4 – 15 LED based on a forward voltage that ranged from 2.6 – 3.5 V. The maximum on time of the control loop has been configured to limit the maximum power delivered. This is illustrated at the top of the output voltage-current transfer function. At the bottom of the curve, even with a short applied to the output, the current is limited to less than 1 A.

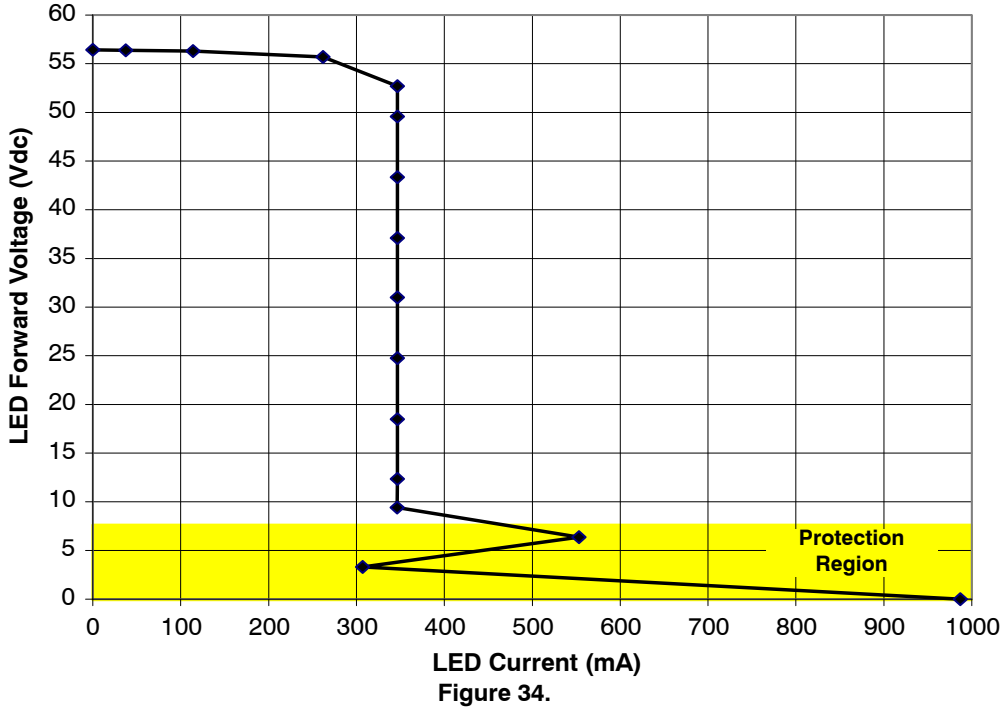

Figure 34.

Figure 35 shows output ripple current for 115 Vac input and 36.9 (12 LED) load operating at 350 mA average. Scale factor is 67 mA per division. The low frequency ripple follows the input twice line frequency rectified sine wave characteristic of single stage converters.

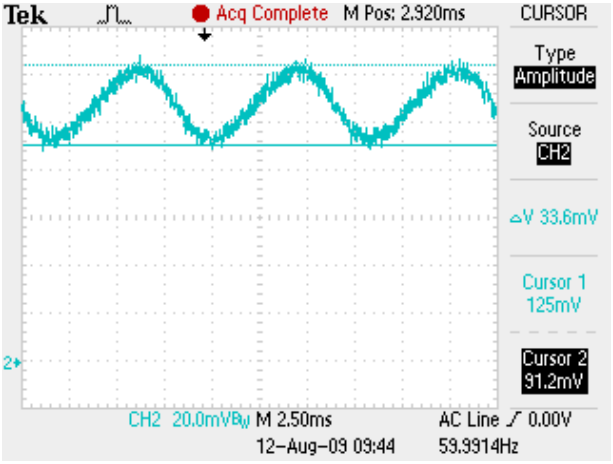

Figure 35. Output Ripple at 115 Vac and 36.9 V, 350 mA Load

Figure 36 shows output ripple current at the main switching frequency. Scale factor is 33 mA per division. This is the signal superimposed over the rectified sine wave ripple component.

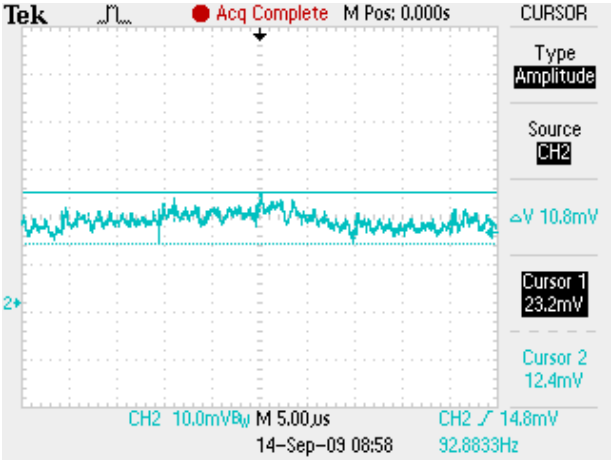

Figure 36. Output Ripple at 115 Vac and 36.9 V, 350 mA Load

Initial start up characteristic is shown in Figure 37 below. Note the higher current limit controlled by the fast feedback loop and the transition to the main average mode feedback control loop. This shows start up at 115 Vac with 36.9 V, 350 mA load. Trace 2 is LED current at 167 mA per division and trace 3 is applied input voltage at 200 V per division.

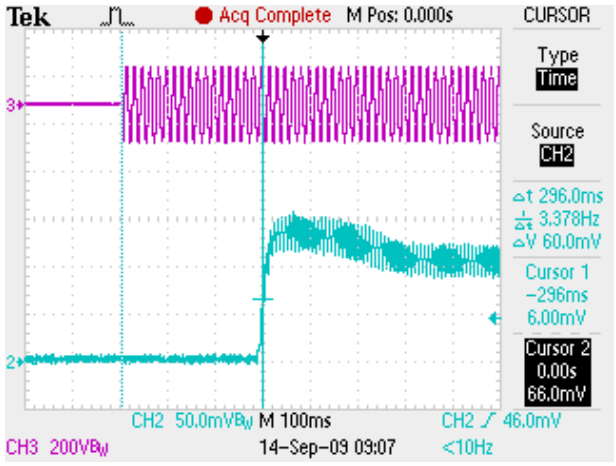

Figure 37. Start up Characteristic with 36.9 V, 350 mA Load

Typical voltage stress on power FET with 36.9 V, 350 mA load and 305 Vac input voltage is shown in Figure 38. Scale factor is 100 V per division.

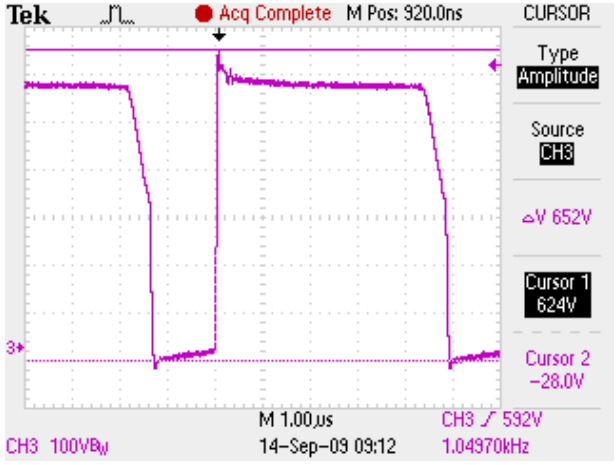

Figure 38. Drain to Source Voltage with 36.9 V, 350 mA Load at 305 Vac Input

Note that while the power supply was designed to meet agency requirements, it has not been submitted for compliance. Standard safety practices should be used when this circuit is energized and in particular when connecting test equipment. During evaluation, input power should be sourced through an isolation transformer.

Additional Application Information and Tools

An evaluation board is available for this 90 – 305 Vac design example. Moreover, for applications where it is desired to dim the LEDs via a TRIAC dimmer, please refer to Application Note AND8448 which explains the steps necessary to configure the NCL30000 for TRIAC dimming. In addition there are two additional TRIAC dimmable reference designs which illustrate a complete design for 90 – 135 Vac or 180 – 265 Vac operation. There is also an Microsoft EXCEL spreadsheet tool available to aid in the design process and assist in developing target winding requirements for the transformer.

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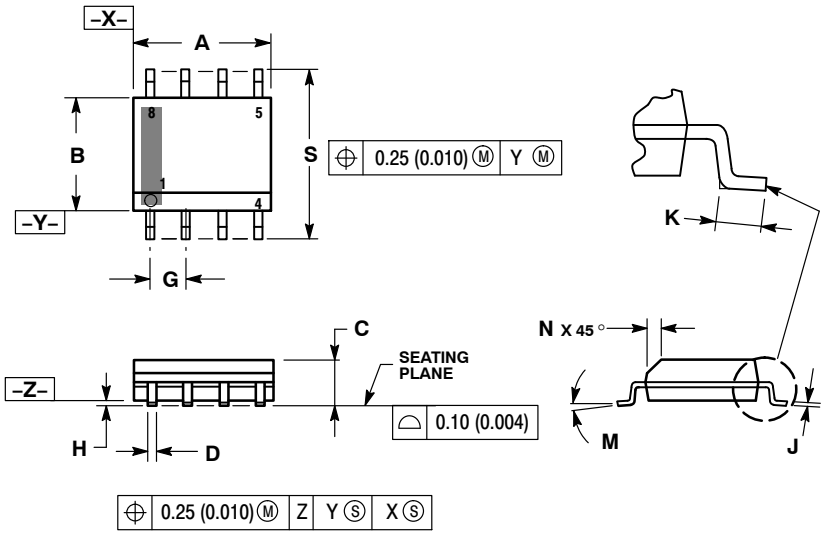
ISSUE AK

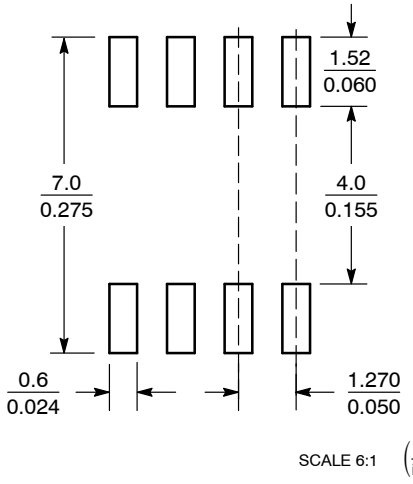
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

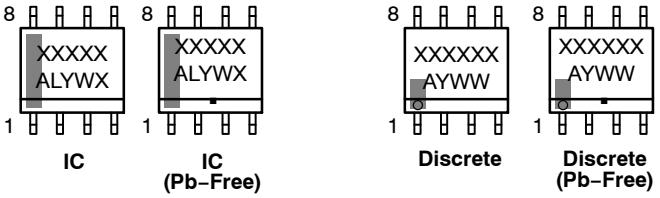
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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