HEF4047B

Monostable/astable multivibrator

Rev. 6 — 17 March 2017 | Product data sheet

1 General description

The HEF4047B is a retriggerable astable multivibrator that can be configured as either a positive-edge or negative-edge triggered monostable multivibrator. The output pulse width is programmed by selection of external components (R_t and C_t). Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2 Features and benefits

2.1 General

- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external resistor and capacitor required

2.2 Monostable multivibrator

- Positive- or negative-edge triggering
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse-width expansion
- Long pulse width possible using small RC components with external counter provision
- Fast recovery time independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

2.3 Astable multivibrator

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
HEF4047BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

4 Functional diagram

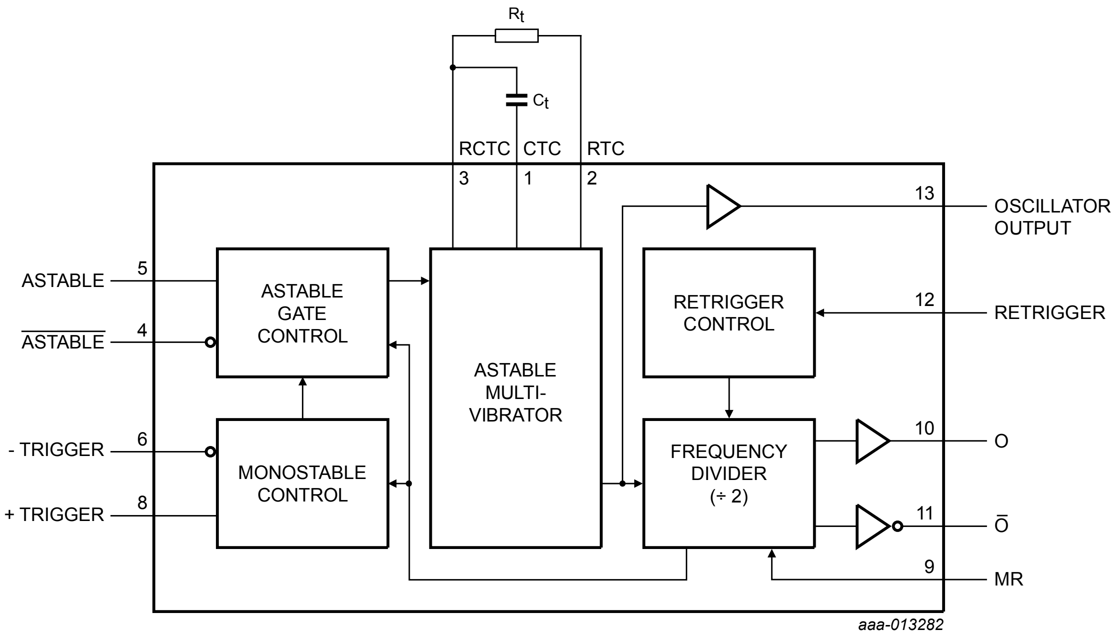
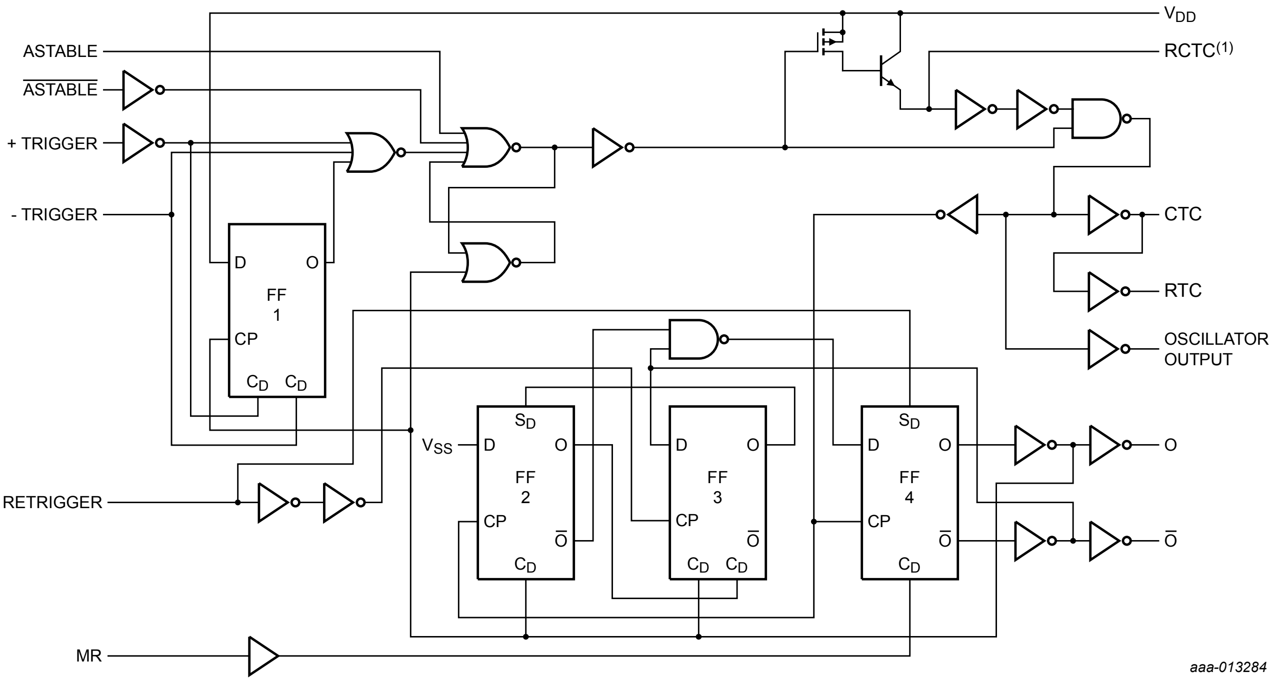


Figure 1. Functional diagram



(1) Special input protection that allows operating input voltages outside the supply voltage lines. Compared to the standard inputprotection pin 3 (RCTC) is more sensitive to static discharge; extra handling precautions are recommended.

Figure 2. Logic diagram

5 Pinning information

5.1 Pinning

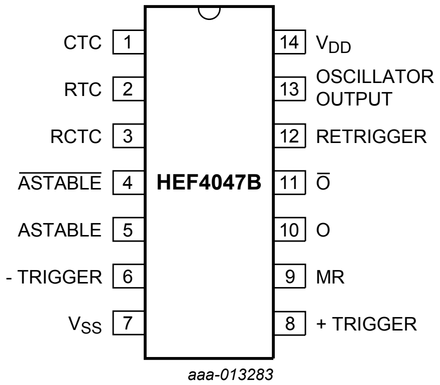


Figure 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
CTC	1	external capacitor connection
RTC	2	external resistor connection
RCTC	3	external capacitor/resistor connection
$\overline{\text{ASTABLE}}$	4	input
ASTABLE	5	input
-TRIGGER	6	input
V_{SS}	7	ground supply voltage
+TRIGGER	8	input
MR	9	master reset input
O	10	output
$\overline{\text{O}}$	11	output
RETRIGGER	12	input
OSCILLATOR OUTPUT	13	oscillator output
V_{DD}	14	supply voltage

6 Functional description

The HEF4047B consists of a gate-able astable multivibrator incorporating logic techniques to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, −TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER and MR (master reset). Buffered outputs are O, $\overline{\text{O}}$ and OSCILLATOR OUTPUT. In all modes of operation an external capacitor (C_t) must be connected between CTC and RCTC, and an external resistor (R_t) must be connected between RTC and RCTC.

A HIGH level on the ASTABLE input enables astable operation. The period of the square wave at O and $\overline{\text{O}}$ outputs is a function of the external components employed. ‘True’ input pulses on the ASTABLE or ‘complement’ pulses on the $\overline{\text{ASTABLE}}$ input, allow the circuit to be used as a gate-able multivibrator. The OSCILLATOR OUTPUT period is half of the O output in the astable mode. However, a 50% duty factor is not guaranteed at this output.

In the monostable mode, positive edge-triggering is accomplished by applying a leading-edge pulse to the +TRIGGER input and a LOW level to the −TRIGGER input. For negative edge-triggering, a trailing-edge pulse is applied to the −TRIGGER and a HIGH level to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading-edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode, the output pulse remains HIGH as long as the input pulse period is shorter than the period determined by the RC components.

An external count down option implements coupling O to an external ‘N’ counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator. A HIGH level on the MR input assures no output pulse during an ON-power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a HIGH level or power-ON reset pulse must be applied to MR, whenever V_{DD} is applied.

7 Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	±10	mA
V_I	input voltage		-0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C			
		SO14 package [1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8 Recommended operating conditions

Table 4. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
V_I	input voltage		0	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{DD} = 5 V	-	3.75	μs/V
		V_{DD} = 10 V	-	0.5	μs/V
		V_{DD} = 15 V	-	0.08	μs/V

9 Static characteristics

Table 5. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V_O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V_O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V_O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
		output transistor OFF; pin 3 at V_{DD} or V_{SS}	15 V	-	±0.3	-	±0.3	-	±1.0	μA
I_{DD}	supply current	I_O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

10 Dynamic characteristics

Table 6. Dynamic characteristics

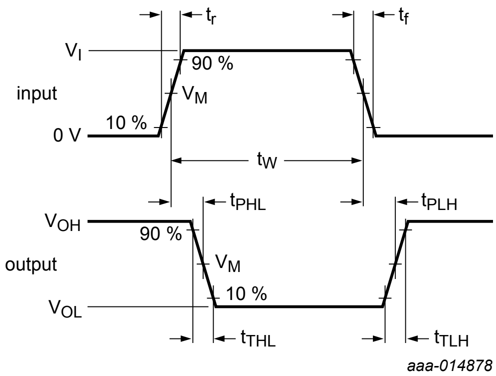
V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified; for waveform and test circuit, see Figure 4 and Figure 5.

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	ASTABLE, $\overline{ASTABLE}$ to OSCILLATOR OUTPUT	5 V	[1]	68 ns + (0.55 ns/pF)C_L	-	95	190	ns
			10 V	[1]	43 ns + (0.23 ns/pF)C_L	-	45	90	ns
			15 V	[1]	22 ns + (0.16 ns/pF)C_L	-	30	60	ns
t_{PLH}	LOW to HIGH propagation delay	ASTABLE, $\overline{ASTABLE}$ to OSCILLATOR OUTPUT	5 V	[1]	58 ns + (0.55 ns/pF)C_L	-	85	170	ns
			10 V		29 ns + (0.23 ns/pF)C_L	-	40	80	ns
			15 V		22 ns + (0.16 ns/pF)C_L	-	30	60	ns
t_{PHL}	HIGH to LOW propagation delay	ASTABLE, $\overline{ASTABLE}$ to O, $\overline{O}$	5 V	[1]	123 ns + (0.55 ns/pF)C_L	-	150	300	ns
			10 V		54 ns + (0.23 ns/pF)C_L	-	65	130	ns
			15 V		42 ns + (0.16 ns/pF)C_L	-	50	100	ns
t_{PLH}	LOW to HIGH propagation delay	ASTABLE, $\overline{ASTABLE}$ to O, $\overline{O}$	5 V	[1]	103 ns + (0.55 ns/pF)C_L	-	130	260	ns
			10 V		49 ns + (0.23 ns/pF)C_L	-	60	120	ns
			15 V		37 ns + (0.16 ns/pF)C_L	-	45	90	ns
t_{PHL}	HIGH to LOW propagation delay	+/-TRIGGER to O, $\overline{O}$	5 V	[1]	133 ns + (0.55 ns/pF)C_L	-	160	320	ns
			10 V		54 ns + (0.23 ns/pF)C_L	-	65	130	ns
			15 V		42 ns + (0.16 ns/pF)C_L	-	50	100	ns
t_{PLH}	LOW to HIGH propagation delay	+/-TRIGGER to O, $\overline{O}$	5 V	[1]	128 ns + (0.55 ns/pF)C_L	-	155	310	ns
			10 V		54 ns + (0.23 ns/pF)C_L	-	65	130	ns
			15 V		42 ns + (0.16 ns/pF)C_L	-	50	100	ns
t_{PHL}	HIGH to LOW propagation delay	+TRIGGER, RETRIGGER to $\overline{O}$	5 V	[1]	38 ns + (0.55 ns/pF)C_L	-	65	130	ns
			10 V		19 ns + (0.23 ns/pF)C_L	-	30	60	ns
			15 V		17 ns + (0.16 ns/pF)C_L	-	25	50	ns
t_{PLH}	LOW to HIGH propagation delay	+TRIGGER, RETRIGGER to O	5 V	[1]	68 ns + (0.55 ns/pF)C_L	-	95	190	ns
			10 V		29 ns + (0.23 ns/pF)C_L	-	40	80	ns
			15 V		22 ns + (0.16 ns/pF)C_L	-	30	60	ns
t_{PHL}	HIGH to LOW propagation delay	MR to O	5 V	[1]	83 ns + (0.55 ns/pF)C_L	-	100	200	ns
			10 V		34 ns + (0.23 ns/pF)C_L	-	45	90	ns
			15 V		27 ns + (0.16 ns/pF)C_L	-	35	70	ns
t_{PLH}	LOW to HIGH propagation delay	MR to $\overline{O}$	5 V	[1]	83 ns + (0.55 ns/pF)C_L	-	100	200	ns
			10 V		34 ns + (0.23 ns/pF)C_L	-	45	90	ns
			15 V		27 ns + (0.16 ns/pF)C_L	-	35	70	ns
t_{THL}	HIGH to LOW output transition time		5 V	[1]	10 ns + (1.0 ns/pF)C_L	-	60	120	ns
			10 V		9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V		6 ns + (0.28 ns/pF)C_L	-	20	40	ns

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_{TLH}	LOW to HIGH output transition time		5 V [1]	10 ns + (1.0 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_W	pulse width	any input except MR	5 V	-	220	110	-	ns
			10 V	-	100	50	-	ns
			15 V	-	70	35	-	ns
		MR HIGH	5 V	-	60	30	-	ns
			10 V	-	30	15	-	ns
			15 V	-	20	10	-	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

10.1 Waveform and test circuit



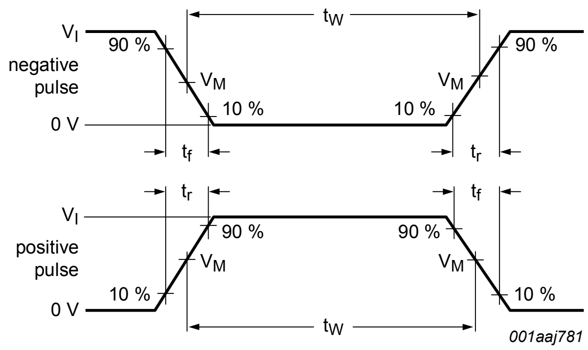
Measurement points are given in Table 7.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

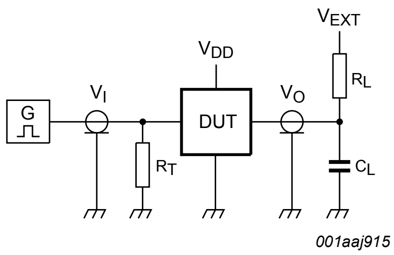
Figure 4. input to output propagation delays, output transition time and pulse width

Table 7. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



a. Input waveform



b. Test circuit

Test and measurement data is given in Table 8.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Figure 5. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input		Load		V_{EXT}
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
5 V to 15 V	V_{DD}	≤ 20 ns	50 pF	1 kΩ	open

11 Application information

Table 9. Functional connections [1]

Function	Pins connected to			Output pulse from pins	Output period or pulse width
	V_{DD}	V_{SS}	input pulse		
Astable multivibrator					
Free running	4, 5, 6, 14	7, 8, 9, 12	-	10, 11, 13	at pins 10, 11; $t_A = 4.40\ R_tC_t$ at pin 13; $t_A = 2.20\ R_tC_t$
True gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	
Complement gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable multivibrator					
Positive edge-triggering	4, 14	5, 6, 7, 9, 12	8	10, 11	at pins 10, 11; $t_M = 2.48\ R_tC_t$
Negative edge-triggering	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External countdown [2]	14	5, 6, 7, 8, 9, 12	-	10, 11	

[1] In all cases, external resistor between pins 2 and 3, external capacitor between pins 1 and 3.

[2] Input pulse to RESET of external counting chip: external counting chip output to pin 4.

11.1 Astable mode design information

11.1.1 Unit-to-unit transfer voltage variations

The following analysis presents worst case variations from unit-to-unit as a function of transfer voltage (V_{TR}) shift for free running (astable) operation.

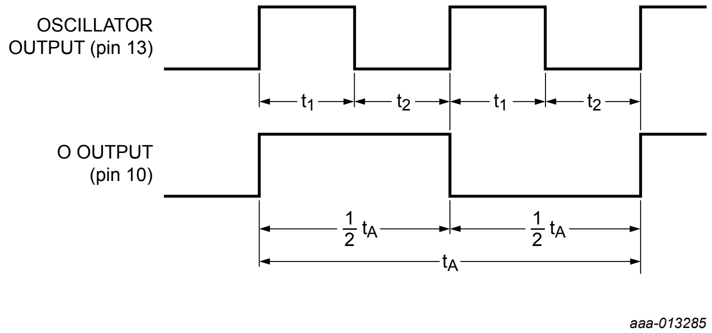


Figure 6. Astable mode waveforms

(1)
$$t_1 = -R_t C_t \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

(2)
$$t_2 = -R_t C_t \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

(3)
$$t_A = 2(t_1 + t_2) = -2R_t C_t \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

, where t_A = astable mode pulse width; see Table 10.

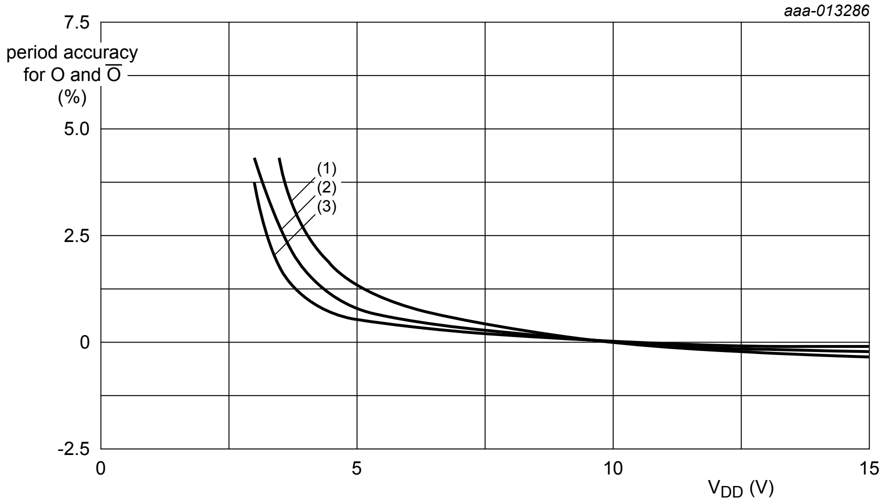
Table 10. Values for astable mode pulse width (t_A)

	V_{TR}			t_A		
	Min	Typ	Max	Min	Typ [1]	Max
V_{DD} = 5 V or 10 V	0.3 × V_{DD}	0.5 × V_{DD}	0.7 × V_{DD}	4.71 R_tC_t	4.40 R_tC_t	4.71 R_tC_t
V_{DD} = 15 V	4 V	0.5 × V_{DD}	11 V	4.84 R_tC_t	4.40 R_tC_t	4.84 R_tC_t

[1] Therefore if t_A = 4.40 R_tC_t is used, the maximum variation is (+7.0%; -0.0%) at 10 V.

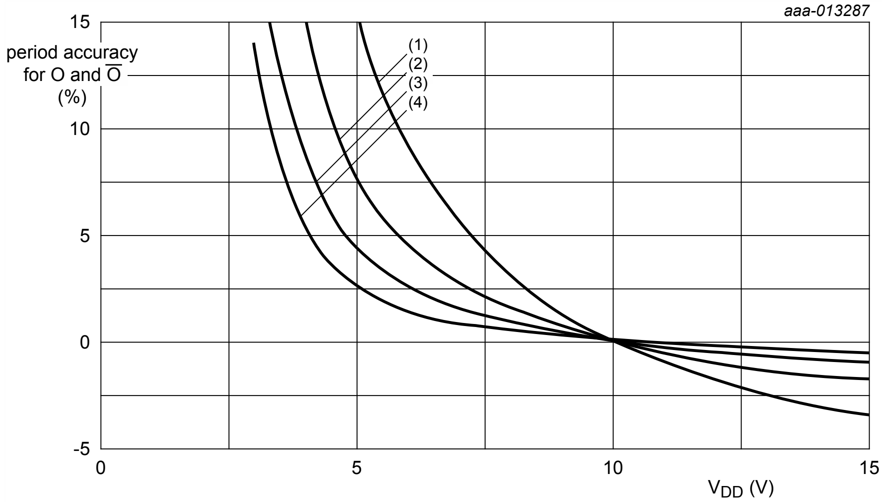
11.1.2 Variations due to changes in V_{DD}

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD}. Typical variations are presented graphically in Figure 7 and Figure 8 with 10 V as a reference.



(1) T_{amb} = 25 °C; f_o = 10 kHz; C_t = 100 pF; R_t = 220 kΩ.
(2) T_{amb} = 25 °C; f_o = 5 kHz; C_t = 100 pF; R_t = 470 kΩ.
(3) T_{amb} = 25 °C; f_o = 1 kHz; C_t = 1000 pF; R_t = 220 kΩ.

Figure 7. Typical O and $\overline{O}$ period accuracy as a function of supply voltage; astable mode.



(1) T_{amb} = 25 °C; f_o = 500 kHz; C_t = 10 pF; R_t = 47 kΩ.
(2) T_{amb} = 25 °C; f_o = 225 kHz; C_t = 100 pF; R_t = 10 kΩ.
(3) T_{amb} = 25 °C; f_o = 100 kHz; C_t = 100 pF; R_t = 22 kΩ.
(4) T_{amb} = 25 °C; f_o = 50 kHz; C_t = 100 pF; R_t = 47 kΩ.

Figure 8. Typical O and $\overline{O}$ period accuracy as a function of supply voltage; astable mode.

11.2 Monostable mode design information

The following analysis presents worst case variations from unit-to-unit as a function of transfer voltage (V_{TR}) shift for one-shot (monostable) operation.

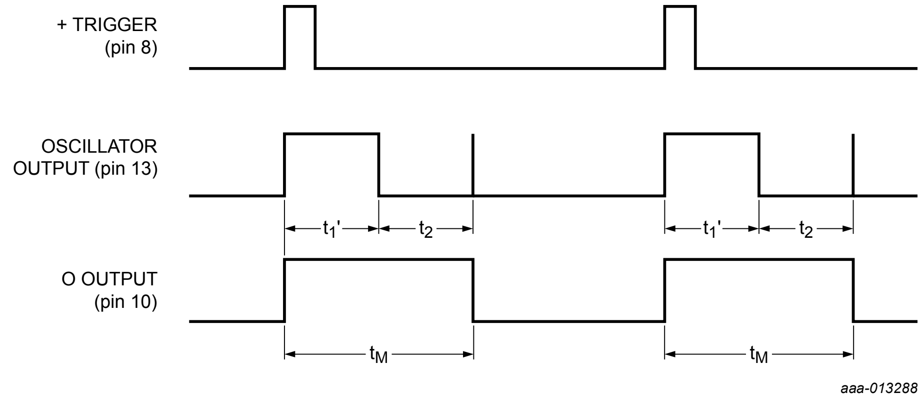


Figure 9. Monostable waveforms.

(4) $$t_1{}' = -R_t C_t \ln\frac{V_{TR}}{2V_{DD}}$$

(5) $$t_M = (t_1{}' + t_2)$$

(6) $$t_M = -R_t C_t \ln\frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

, where t_M = monostable mode pulse width; see table Table 11.

Table 11. Values for monostable mode pulse width (t_M)

	V_{TR}			t_M		
	Min	Typ	Max	Min	Typ [1]	Max
V_{DD} = 5 V or 10 V	0.3 × V_{DD}	0.5 × V_{DD}	0.7 × V_{DD}	2.78 R_tC_t	2.48 R_tC_t	2.52 R_tC_t
V_{DD} = 15 V	4 V	0.5 × V_{DD}	11 V	2.88 R_tC_t	2.48 R_tC_t	2.56 R_tC_t

[1] In the astable mode, the first positive half cycle has a duration of t_M: succeeding durations are $\frac{1}{2}$ t_A. Therefore if t_M = 2.48 R_tC_t is used, the maximum variation is (+12%; -0.0%) at 10 V.

11.2.1 Retrigger mode operation

The HEF4047B can be used in the retrigger mode to extend the output pulse duration. It can also be used to compare the frequency of an input signal with the frequency of the internal oscillator. In the retrigger mode, the input pulse is applied to pins 8 and 12, and the output is taken from pin 10 or 11. Normal monostable action is obtained when one retrigger pulse is applied (see Figure 10). Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (output O), terminates at some variable time, t_D, after the termination of the last retrigger pulse. t_D is variable because t_{RE} (output O) terminates after the second positive edge of the oscillator output appears at flip-flop 4.

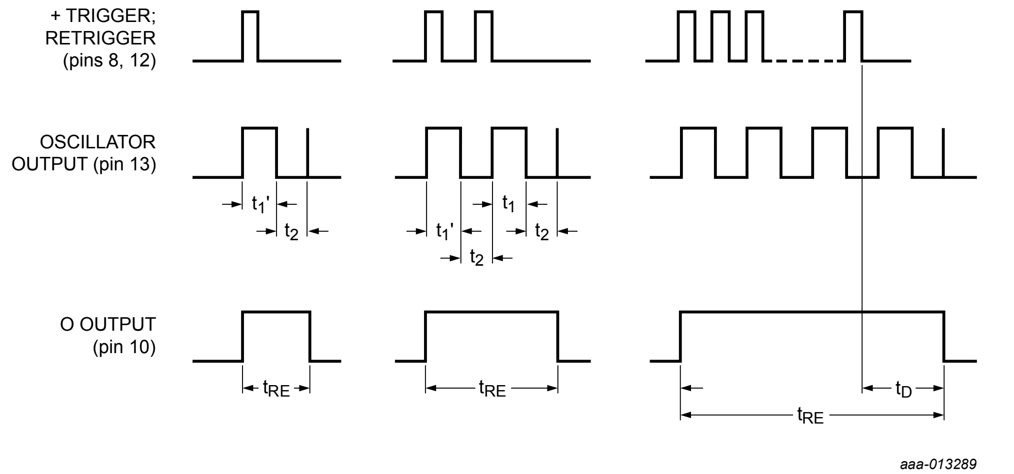


Figure 10. Retrigger mode waveforms.

11.2.2 External counter option

The use of external counting circuitry extends time t_M by any amount. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Figure 11.

The pulse duration at the output is:

$$t_{ext} = (N - 1)(t_A) + (t_M + 1/2\ t_A) \tag{7}$$

Where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

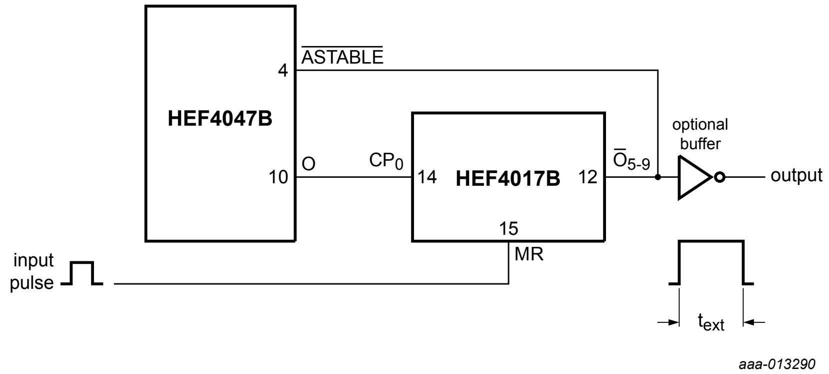


Figure 11. Implementation of external counter option.

11.2.3 Timing component limitations

The capacitor used in the circuit should be non-polarized and have low leakage (that is the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R_t or C_t value to maintain oscillation. However, for accuracy, C_t must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R_t must be much larger than the LOCMOS 'ON' resistance in series with it, which typically is hundreds of ohms.

The recommended values for R_t and C_t to comply with previously calculated formulae without trimming should be:

- $C_t \geq 100$ pF, up to any practical value
- 10 kΩ ≤ R_t ≤ 1 MΩ

11.2.4 Power consumption

In the standby mode (monostable or astable), power dissipation is a function of leakage current in the circuit. For dynamic operation, the power required to charge the external timing capacitor C_t is shown in the following formulae:

Astable mode:

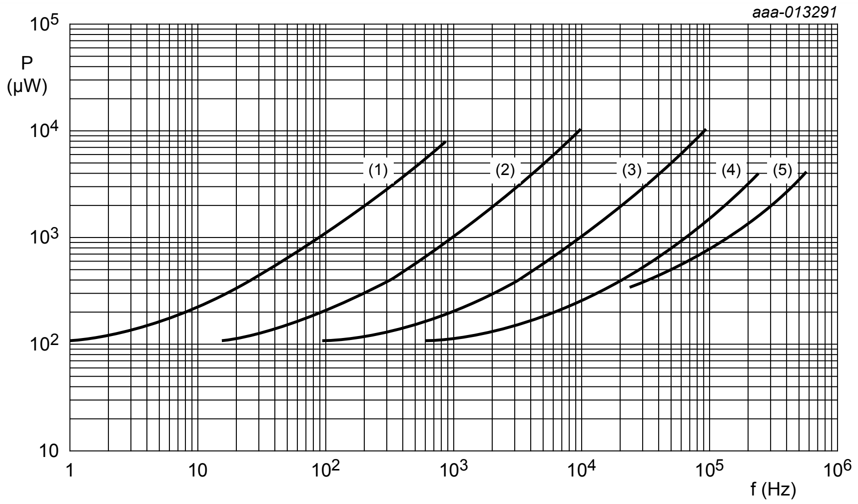
(8) $$P = 2C_tV^2f \qquad (\text{f at output pin 13})$$

(9) $$P = 4C_tV^2f \qquad (\text{f at output pins 10 and 11})$$

Monostable mode:

(10) $$P = \frac{(2.9C_tV^2)(\text{duty cycle})}{T} \qquad (\text{f at output pins 10 and 11})$$

Because the power dissipation does not depend on R_t, a design for minimum power dissipation would be a small value of C_t. The value of R would depend on the desired period (within the limitations discussed previously). Typical power consumption in astable mode is shown in Figure 12, Figure 13 and Figure 14.



V_{DD} = 5 V.

(1) C_t = 100 nF.

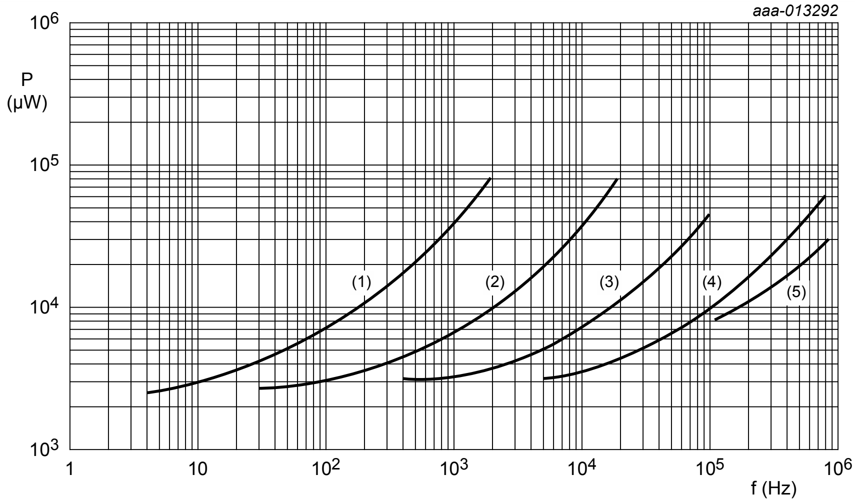
(2) C_t = 10 nF.

(3) C_t = 1 nF.

(4) C_t = 100 pF.

(5) C_t = 10 pF.

Figure 12. Power consumption as a function of the output frequency at O or $\overline{O}$; astable mode.



V_{DD} = 10 V.

(1) C_t = 100 nF.

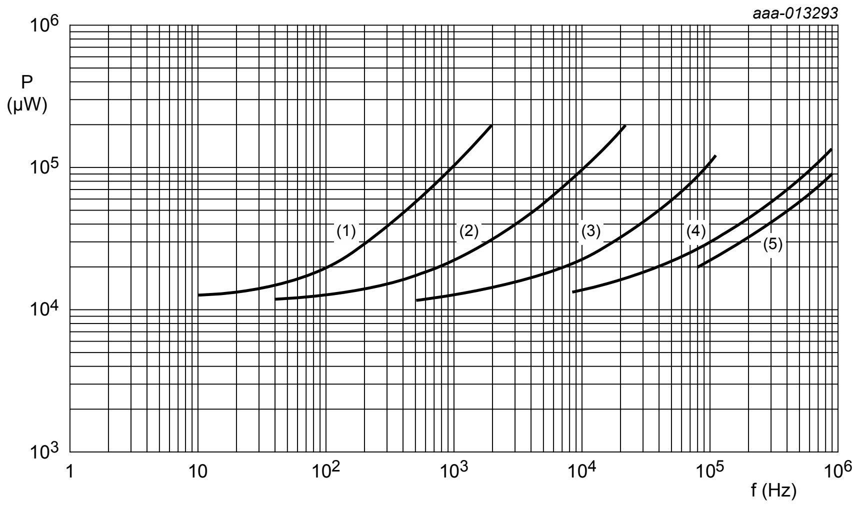
(2) C_t = 10 nF.

(3) C_t = 1 nF.

(4) C_t = 100 pF.

(5) C_t = 10 pF.

Figure 13. Power consumption as a function of the output frequency at O or $\overline{O}$; astable mode.



V_{DD} = 15 V.

(1) C_t = 100 nF.

(2) C_t = 10 nF.

(3) C_t = 1 nF.

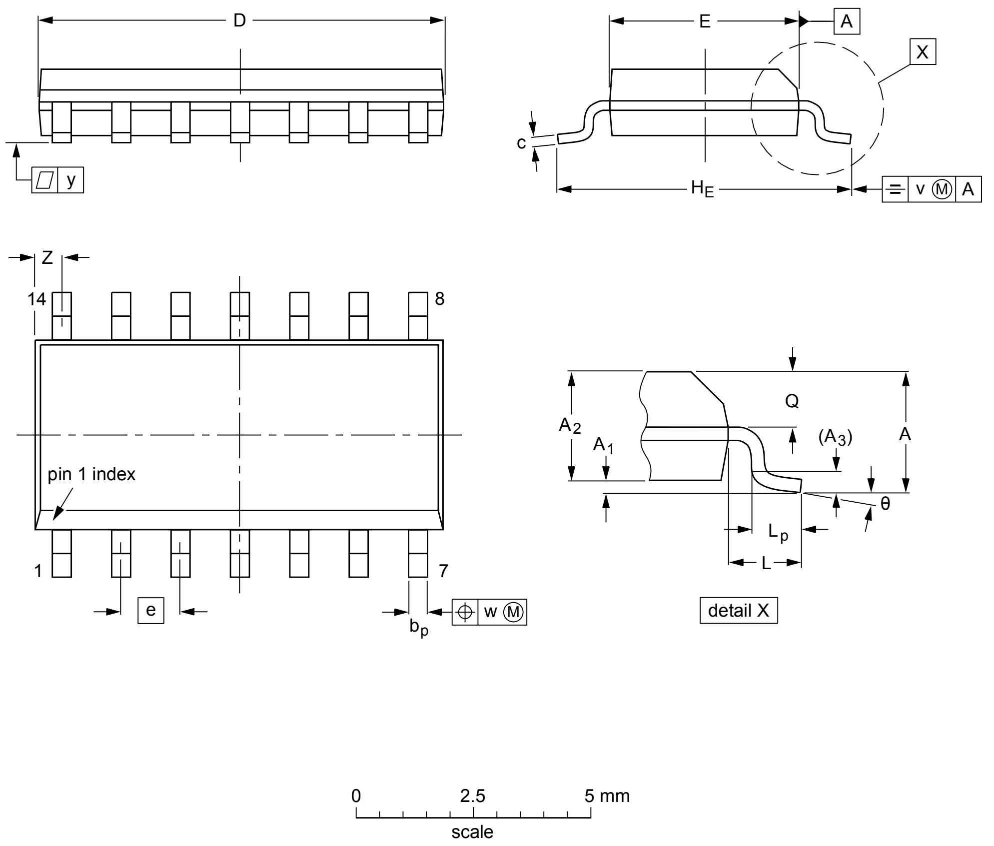
(4) C_t = 100 pF.

(5) C_t = 10 pF.

Figure 14. Power consumption as a function of the output frequency at O or $\overline{O}$; astable mode.

12 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Figure 15. Package outline SOT108-1 (SO14)

13 Abbreviations

Table 12. Abbreviations

Acronym	Description
DUT	Device Under Test

14 Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4047B v.6	20170317	Product data sheet	-	HEF4047B v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
HEF4047B v.5	20151216	Product data sheet	-	HEF4047B v.4
Modifications:	• Type number HEF4047BP (SOT27-1) removed.			
HEF4047B v.4	20140915	Product data sheet	-	HEF4047B_CVN_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
HEF4047B_CVN_3	19950101	Product specification	-	-

15 Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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