

MC14076B

4-Bit D-Type Register with Three-State Outputs

The MC14076B 4-Bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated output-disable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master reset is provided to clear all four flip-flops simultaneously independent of the clock or disable inputs.

Features

- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- Four Bus Buffer Registers
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|----------------------|---|------------------------|------|
| V_{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V_{in} , V_{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in} , I_{out} | Input or Output Current (DC or Transient) per Pin | ± 10 | mA |
| P_D | Power Dissipation, per Package (Note 1) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | °C |
| T_{stg} | Storage Temperature Range | -65 to +150 | °C |
| T_L | Lead Temperature (8-Second Soldering) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

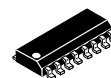
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



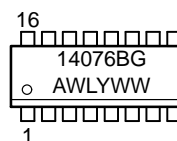
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SOIC-16
D SUFFIX
CASE 751B

MARKING DIAGRAM



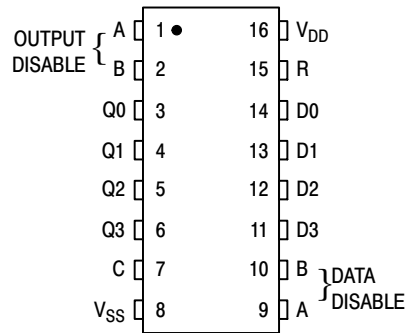
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

ORDERING INFORMATION

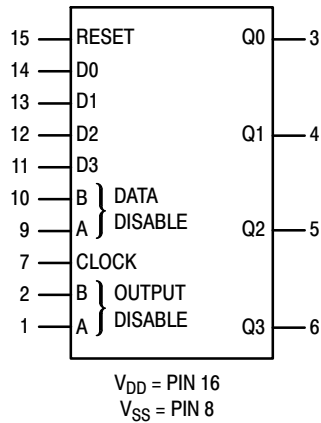
See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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PIN ASSIGNMENT



BLOCK DIAGRAM



FUNCTION TABLE

| Inputs | | | | | Output Q |
|--------|---|--------------|---|-----------|-------------|
| Reset | Clock | Data Disable | | Data D | |
| | | A | B | | |
| 1 | X | X | X | X | 0 |
| 0 | 0 | X | X | X | Q_n |
| 0 |  | 1 | X | X | Q_n |
| 0 |  | X | 1 | X | Q_n |
| 0 |  | 0 | 0 | 0 | 0 |
| 0 |  | 0 | 0 | 1 | 1 |

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.
X = Don't Care.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | -55°C | | 25°C | | | 125°C | | Unit |
|--|------------------------------|------------------------|--|------|-------|-----------------|------|-------|------|------|
| | | | Min | Max | Min | Typ (Note 2) | Max | Min | Max | |
| Output Voltage V _{in} = V _{DD} or 0 | "0" Level V _{OL} | 5.0 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| | | 10 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| | | 15 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| | "1" Level V _{OH} | 5.0 | 4.95 | – | 4.95 | 5.0 | – | 4.95 | – | Vdc |
| | | 10 | 9.95 | – | 9.95 | 10 | – | 9.95 | – | |
| | | 15 | 14.95 | – | 14.95 | 15 | – | 14.95 | – | |
| Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) | "0" Level V _{IL} | 5.0 | – | 1.5 | – | 2.25 | 1.5 | – | 1.5 | Vdc |
| | | 10 | – | 3.0 | – | 4.50 | 3.0 | – | 3.0 | |
| | | 15 | – | 4.0 | – | 6.75 | 4.0 | – | 4.0 | |
| | "1" Level V _{IH} | 5.0 | 3.5 | – | 3.5 | 2.75 | – | 3.5 | – | Vdc |
| | | 10 | 7.0 | – | 7.0 | 5.50 | – | 7.0 | – | |
| | | 15 | 11 | – | 11 | 8.25 | – | 11 | – | |
| Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) | Source I _{OH} | 5.0 | –3.0 | – | –2.4 | –4.2 | – | –1.7 | – | mAdc |
| | | 5.0 | –0.64 | – | –0.51 | –0.88 | – | –0.36 | – | |
| | | 10 | –1.6 | – | –1.3 | –2.25 | – | –0.9 | – | |
| | | 15 | –4.2 | – | –3.4 | –8.8 | – | –2.4 | – | |
| | Sink I _{OL} | 5.0 | 0.64 | – | 0.51 | 0.88 | – | 0.36 | – | mAdc |
| | | 10 | 1.6 | – | 1.3 | 2.25 | – | 0.9 | – | |
| | | 15 | 4.2 | – | 3.4 | 8.8 | – | 2.4 | – | |
| Input Current | I _{in} | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±1.0 | μAdc |
| Input Capacitance (V _{in} = 0) | C _{in} | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current (Per Package) | I _{DD} | 5.0 | – | 5.0 | – | 0.005 | 5.0 | – | 150 | μAdc |
| | | 10 | – | 10 | – | 0.010 | 10 | – | 300 | |
| | | 15 | – | 20 | – | 0.015 | 20 | – | 600 | |
| Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching) | I _T | 5.0 10 15 | I _T = (0.75 μA/kHz) f + I _{DD} I _T = (1.50 μA/kHz) f + I _{DD} I _T = (2.25 μA/kHz) f + I _{DD} | | | | | | | μAdc |
| Three-State Leakage Current | I _{TL} | 15 | – | ±0.1 | – | ±0.0001 | ±0.1 | – | ±3.0 | μAdc |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

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SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V_{DD} Vdc | Min | Typ (Note 6) | Max | Unit |
|--|--------------------|--|--------------------------------|--|--|---------------|
| Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | t_{TLH}, t_{THL} | 5.0 10 15 | – – – | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time Clock to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ Reset to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ | t_{PLH}, t_{PHL} | 5.0 10 15 5.0 10 15 | – – – – – – | 300 125 90 300 125 90 | 600 250 180 600 250 180 | ns |
| 3-State Propagation Delay, Output “1” or “0” to High Impedance | t_{PHZ}, t_{PLZ} | 5.0 10 15 | – – – | 150 60 45 | 300 120 90 | ns |
| 3-State Propagation Delay, High Impedance to “1” or “0” Level | t_{PZH}, t_{PZL} | 5.0 10 15 | – – – | 200 80 60 | 400 160 120 | ns |
| Clock Pulse Width | t_{WH} | 5.0 10 15 | 260 110 80 | 130 55 40 | – – – | ns |
| Reset Pulse Width | t_{WH} | 5.0 10 15 | 370 150 110 | 185 75 55 | – – – | ns |
| Data Setup Time | t_{su} | 5.0 10 15 | 30 10 4 | 15 5 2 | – – – | ns |
| Data Hold Time | t_h | 5.0 10 15 | 130 60 50 | 65 30 25 | – – – | ns |
| Data Disable Setup Time | t_{su} | 5.0 10 15 | 220 80 50 | 110 40 25 | – – – | ns |
| Clock Pulse Rise and Fall Time | t_{TLH}, t_{THL} | 5.0 10 15 | – – – | – – – | 15 5 4 | μs |
| Clock Pulse Frequency | f_{cl} | 5.0 10 15 | – – – | 3.6 9.0 12 | 1.8 4.5 6.0 | MHz |

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

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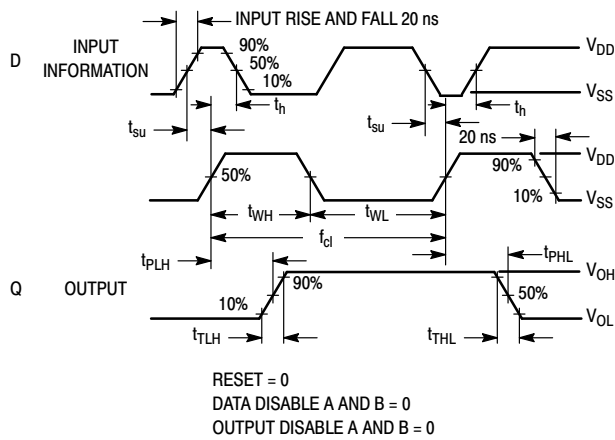


Figure 1. Timing Diagram

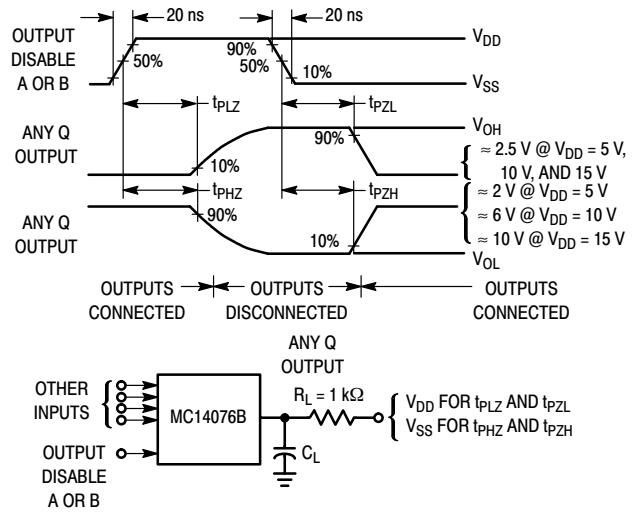
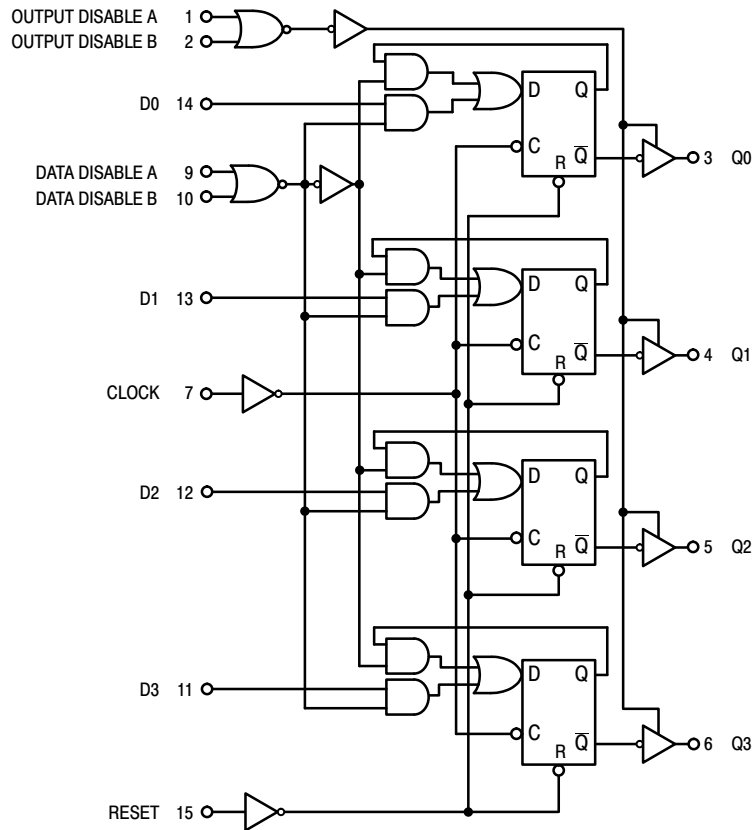


Figure 2. Three-State Propagation Delay Waveshape and Circuit

EQUIVALENT FUNCTIONAL BLOCK DIAGRAM



MC14076B

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|----------------|----------------------|--------------------------|
| MC14076BDG | SOIC-16 (Pb-Free) | 48 Units / Rail |
| MC14076BDR2G | SOIC-16 (Pb-Free) | 2500 Units / Tape & Reel |
| NLV14076BDR2G* | SOIC-16 (Pb-Free) | 2500 Units / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

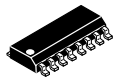
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

ON



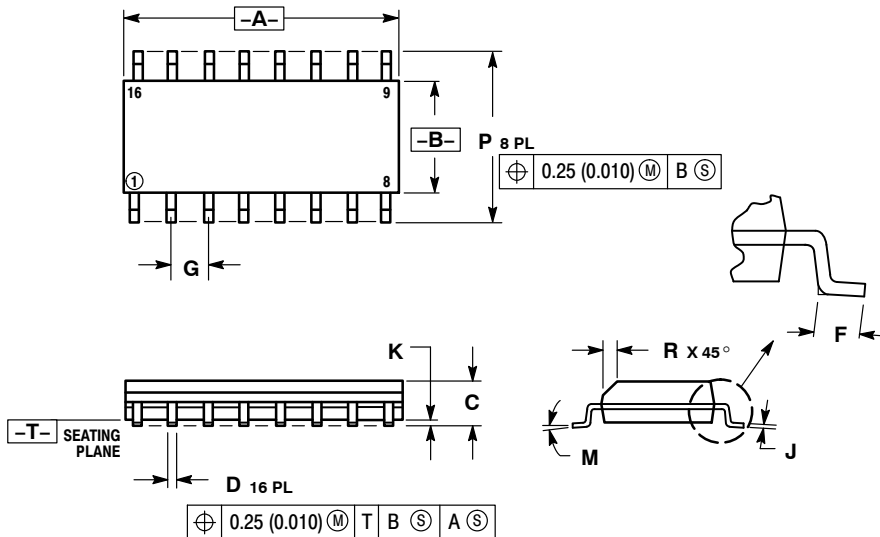
SCALE 1:1

SOIC-16

CASE 751B-05

ISSUE K

DATE 29 DEC 2006



NOTES:

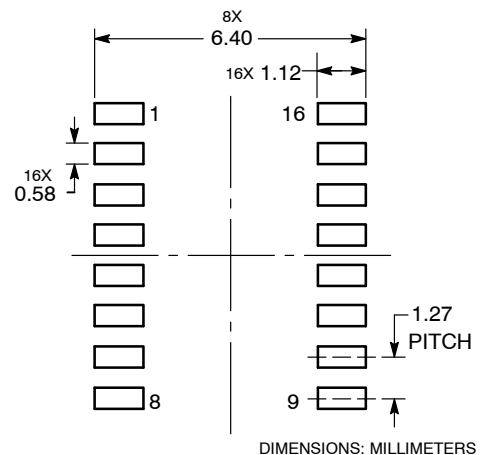
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| E | 0.40 | 1.25 | 0.016 | 0.049 |
| F | 1.27 BSC | | 0.050 BSC | |
| G | 0.19 | 0.25 | 0.008 | 0.009 |
| H | 0.10 | 0.25 | 0.004 | 0.009 |
| I | 0° | 7° | 0° | 7° |
| J | 5.80 | 6.20 | 0.229 | 0.244 |
| K | 0.25 | 0.50 | 0.010 | 0.019 |

| | | | |
|-------------------|-------------------|--------------------------|--------------------------|
| STYLE 1: | STYLE 2: | STYLE 3: | STYLE 4: |
| PIN 1. COLLECTOR | PIN 1. CATHODE | PIN 1. COLLECTOR, DYE #1 | PIN 1. COLLECTOR, DYE #1 |
| 2. BASE | 2. ANODE | 2. BASE, #1 | 2. COLLECTOR, #1 |
| 3. EMITTER | 3. NO CONNECTION | 3. EMITTER, #1 | 3. COLLECTOR, #2 |
| 4. NO CONNECTION | 4. CATHODE | 4. COLLECTOR, #1 | 4. COLLECTOR, #2 |
| 5. EMITTER | 5. CATHODE | 5. COLLECTOR, #2 | 5. COLLECTOR, #3 |
| 6. BASE | 6. NO CONNECTION | 6. BASE, #2 | 6. COLLECTOR, #3 |
| 7. COLLECTOR | 7. ANODE | 7. EMITTER, #2 | 7. COLLECTOR, #4 |
| 8. COLLECTOR | 8. CATHODE | 8. COLLECTOR, #2 | 8. COLLECTOR, #4 |
| 9. BASE | 9. CATHODE | 9. COLLECTOR, #3 | 9. BASE, #4 |
| 10. EMITTER | 10. ANODE | 10. BASE, #3 | 10. EMITTER, #4 |
| 11. NO CONNECTION | 11. NO CONNECTION | 11. EMITTER, #3 | 11. BASE, #3 |
| 12. EMITTER | 12. CATHODE | 12. COLLECTOR, #3 | 12. EMITTER, #3 |
| 13. BASE | 13. CATHODE | 13. COLLECTOR, #4 | 13. BASE, #2 |
| 14. COLLECTOR | 14. NO CONNECTION | 14. BASE, #4 | 14. EMITTER, #2 |
| 15. EMITTER | 15. ANODE | 15. EMITTER, #4 | 15. BASE, #1 |
| 16. COLLECTOR | 16. CATHODE | 16. COLLECTOR, #4 | 16. EMITTER, #1 |

| | | |
|----------------------|----------------|---------------------------|
| STYLE 5: | STYLE 6: | STYLE 7: |
| PIN 1. DRAIN, DYE #1 | PIN 1. CATHODE | PIN 1. SOURCE N-CH |
| 2. DRAIN, #1 | 2. CATHODE | 2. COMMON DRAIN (OUTPUT) |
| 3. DRAIN, #2 | 3. CATHODE | 3. COMMON DRAIN (OUTPUT) |
| 4. DRAIN, #2 | 4. CATHODE | 4. GATE P-CH |
| 5. DRAIN, #3 | 5. CATHODE | 5. COMMON DRAIN (OUTPUT) |
| 6. DRAIN, #3 | 6. CATHODE | 6. COMMON DRAIN (OUTPUT) |
| 7. DRAIN, #4 | 7. CATHODE | 7. COMMON DRAIN (OUTPUT) |
| 8. DRAIN, #4 | 8. CATHODE | 8. SOURCE P-CH |
| 9. GATE, #4 | 9. ANODE | 9. SOURCE P-CH |
| 10. SOURCE, #4 | 10. ANODE | 10. COMMON DRAIN (OUTPUT) |
| 11. GATE, #3 | 11. ANODE | 11. COMMON DRAIN (OUTPUT) |
| 12. SOURCE, #3 | 12. ANODE | 12. COMMON DRAIN (OUTPUT) |
| 13. GATE, #2 | 13. ANODE | 13. GATE N-CH |
| 14. SOURCE, #2 | 14. ANODE | 14. COMMON DRAIN (OUTPUT) |
| 15. GATE, #1 | 15. ANODE | 15. COMMON DRAIN (OUTPUT) |
| 16. SOURCE, #1 | 16. ANODE | 16. SOURCE N-CH |

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

| | | |
|------------------|-------------|---|
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