Prioritized PowerPath™ Controller

FEATURES

- **Selects Highest Priority Supply from Three Inputs**
- **Blocks Reverse and Cross Conduction Currents**
- **Wide Operating Voltage Range: 2.5V to 36V**
- **–42V Protection Against Reverse Battery Connection**
- Fast Switchover Minimizes Output Voltage Droop
- Low 28µA Operating Current
- <1µA Current Draw from Supplies Less than V_{OUT}
- 1.5% Input Overvoltage/Undervoltage Protection
- Adjustable Overvoltage/Undervoltage Hysteresis
- P-Channel MOSFET Gate Protection Clamp
- Cascadable for Additional Input Supplies
- 24-Lead Narrow SSOP and 4mm × 4mm QFN Packages

APPLICATIONS

- Industrial Handheld Instruments
- High Availability Systems
- Battery Backup Systems
- Servers and Computer Peripherals

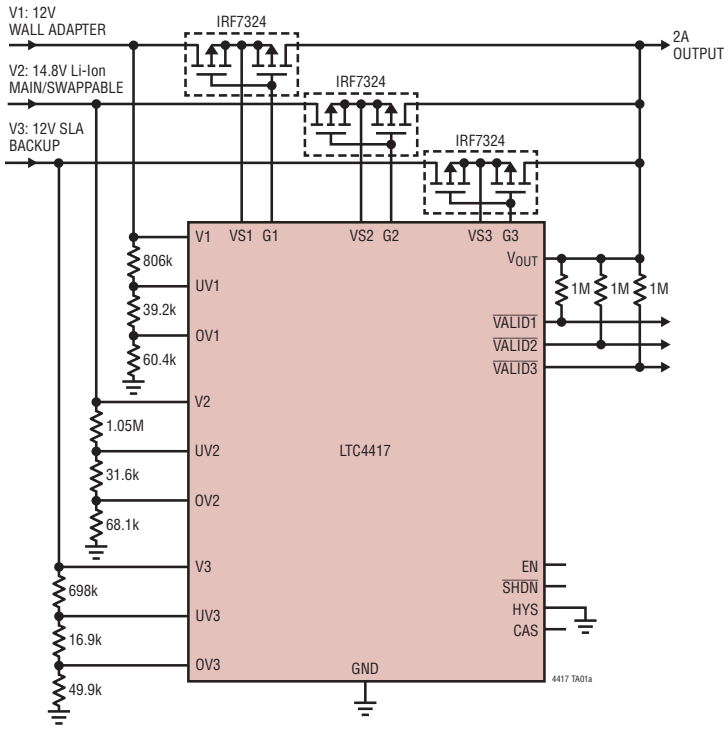
DESCRIPTION

The LTC®4417 connects one of three valid power supplies to a common output based on priority. Priority is defined by pin assignment, with V1 assigned the highest priority and V3 the lowest priority. A power supply is defined as valid when its voltage has been within its overvoltage (OV) and undervoltage (UV) window continuously for at least 256ms. If the highest priority valid input falls out of the OV/UV window, the channel is immediately disconnected and the next highest priority valid input is connected to the common output. Two or more LTC4417s can be cascaded to provide switchover between more than three inputs.

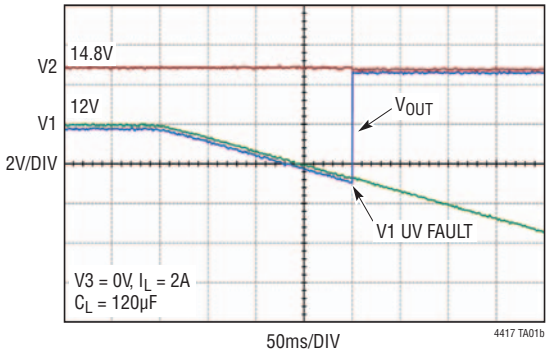
The LTC4417 incorporates fast non-overlap switching circuitry to prevent both reverse and cross conduction while minimizing output droop. The gate driver includes a 6V clamp to protect external MOSFETs. A controlled output ramp feature minimizes start-up inrush current. Open drain $\overline{\text{VALID}}$ outputs indicate the input supplies have been within their OV/UV window for 256ms.

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TYPICAL APPLICATION



Priority Switching from 12V V1 to 14.8V V2



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages
- V1, V2, V3 ..... –42V to 42V
- V_{OUT}, VS1, VS2, VS3 ..... –0.3V to 42V

Voltage from V1, V2, V3 to V_{OUT} ..... –84V to 42V

Voltage from VS1, VS2, VS3 to G1, G2, G3 ..... –0.3V to 7.5V

Input Voltages
- EN, $\overline{SHDN}$ ..... –0.3V to 42V
- OV1, OV2, OV3, UV1, UV2, UV3 ..... –0.3V to 6V
- HYS ..... –0.3V to 1V

Input Currents
- OV1, OV2, OV3, UV1, UV2, UV3, HYS ..... –3mA

Output Voltages
- $\overline{VALID1}$, $\overline{VALID2}$, $\overline{VALID3}$ ..... –0.3V to 42V
- CAS ..... –0.3V to 6V

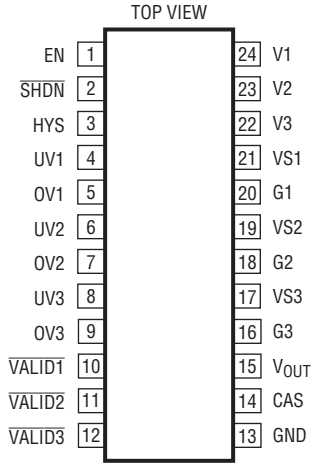
Output Currents
- $\overline{VALID1}$, $\overline{VALID2}$, $\overline{VALID3}$, CAS 2mA

Operating Ambient Temperature Range
- LTC4417C ..... 0°C to 70°C
- LTC4417I ..... –40°C to 85°C
- LTC4417H ..... –40°C to 125°C

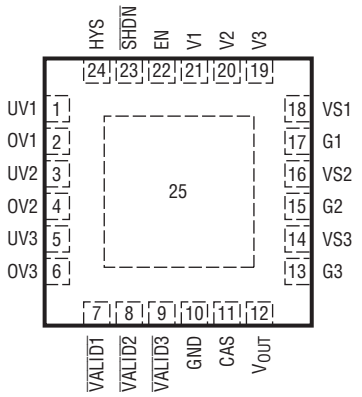
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature
- GN Package (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



GN PACKAGE
24-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 85°C/W, θ_{JC} = 30°C/W



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 47°C/W, θ_{JC} = 4.5°C/W
EXPOSED PAD (PIN 25) PCB GND CONNECTION OPTIONAL

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4417CGN#PBF	LTC4417CGN#TRPBF	LTC4417GN	24-Lead Narrow Plastic SSOP	0°C to 70°C
LTC4417IGN#PBF	LTC4417IGN#TRPBF	LTC4417GN	24-Lead Narrow Plastic SSOP	–40°C to 85°C
LTC4417HGN#PBF	LTC4417HGN#TRPBF	LTC4417GN	24-Lead Narrow Plastic SSOP	–40°C to 125°C
LTC4417CUF#PBF	LTC4417CUF#TRPBF	4417	24-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C
LTC4417IUF#PBF	LTC4417IUF#TRPBF	4417	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC4417HUF#PBF	LTC4417HUF#TRPBF	4417	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. For all tests, V1 = VS1, V2 = VS2, V3 = VS3. Unless otherwise noted, V1 = V2 = V3 = V_{OUT} = 12V, HYS = GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Start-Up							
V1-V3,V_{OUT}	V1 to V3,V_{OUT} Operating Supply Range		●	2.5		36	V
$I_{V1-V3,VOUT(EN)}$	Total Supply Current with Channels Enabled	V1 = 5V, V2 = 12V, V3 = 2.5V, V_{OUT} = 4V, (Notes 3, 4)	●		28	78	µA
$I_{V1-V3(\overline{EN})}$	Total Supply Current with Channels Disabled	V1 = 5V, V2 = 12V, V3 = 2.5V, V_{OUT} = EN = 0V, (Notes 3, 4)	●		31	93	µA
$I_{V1-V3(\overline{SHDN})}$	Total Supply Current When Shutdown	V1 = 5V, V2 = 12V, V3 = 2.5V, V_{OUT} = $\overline{SHDN}$ = 0V, (Notes 3, 4)	●		15.4	84	µA
I_{VOUT}	V_{OUT} Supply Current	V1 = 5V, V2 = 12V, V3 = 2.5V, V_{OUT} = 4V	●		14	30	µA
$I_{PRIORITY}$	Current from Highest V1 to V3 Priority Input Source (V1)	V1 = 5V, V2 = 12V, V3 = 2.5V, V_{OUT} = 4V V1 = 5V, V2 = 12V, V3 = 2.5V, V_{OUT} = EN = 0V	● ●		2.6 20	6 45	µA µA
$I_{HIGHEST}$	Current from Highest V1 to V3 Voltage Input Source	V1 = 5V, V2 = 12V, V3 = 2.5V, V_{OUT} = 4V, (Note 3, 4)	●		11	72	µA
		V1 = 5V, V2 = 12V, V3 = 2.5V, V_{OUT} = EN = 0V, $\overline{SHDN}$ = 0V, (Note 3, 4)	●		15	80	µA
I_{LOWER}	Current from V1 to V3 Input Voltage Sources Lower than V_{OUT}	V1 = 5V, V2 = 12V, V3 = 2.5V, V_{OUT} = 4V Not Highest Valid Priority		–5	0.2	1	µA
Gate Control							
ΔV_G	Open (VS – VG) Clamp Voltage	V_{OUT} = 11V, G1 to G3 = Open	●	5.4	6.2	6.7	V
$\Delta V_{G(SOURCE)}$	Sourcing (VS – VG) Clamp Voltage	V_{OUT} = 11V, I = –10µA	●	5.8	6.6	7	V
$\Delta V_{G(SINK)}$	Sinking (VS – VG) Clamp Voltage	V_{OUT} = 11V, I = 10µA	●	4.5	5.2	6	V
$\Delta V_{G(OFF)}$	G1 to G3 Off (VS – VG) Threshold	V1 = V2 = V3 = 2.8V, V_{OUT} = 2.6V, G1 to G3 Rising Edge	●	0.12	0.35	0.6	V
$\Delta V_{G(SLEW,ON)}$	G1 to G3 Pull-Down Slew Rate	V_{OUT} = 11V, C_{GATE} = 10nF (Note 5)	●	4	9	20	V/µs
$\Delta V_{G(SLEW,OFF)}$	G1 to G3 Pull-Up Slew Rate	V_{OUT} = 11V, C_{GATE} = 10nF (Note 6)	●	7.5	13	22	V/µs
$I_{G(DN)}$	G1 to G3 Low Pull-Down Current	V_{OUT} = 2.6V, V1 to V3 = 2.8V, (G1 to G3) = ΔV_G + 300mV		0.8	2	7	µA
$R_{G(OFF)}$	G1 to G3 OFF Resistance	V_{OUT} = 4V, V1 to V3 = 5V, I_G = –10mA	●	9	16	26	Ω
V_{REV}	Reverse Voltage Threshold	Measure (V1 to V3) – V_{OUT}, V_{OUT} Falling	●	30	120	200	mV
$t_{G(SWITCHOVER)}$	Pin Break-Before-Make Time	V_{OUT} = 11V, C_{GATE} = 10nF, (Note 7)	●	0.7	2	3	µs
$t_{pG(\overline{SHDN})}$	G1 to G3 Turn-Off Delay From $\overline{SHDN}$	V_{OUT} = 11V, Falling Edge $\overline{SHDN}$ to (G1 to G3) = (VS1 to VS3) – 3V, C_{GATE} = 10nF	●	20	50	100	µs
$t_{pG(EN,OFF)}$	G1 to G3 Turn-Off Delay From EN	V_{OUT} = 11V, Falling EN Edge to (G1 to G3) = (VS1 to VS3) – 3V, C_{GATE} = 10nF	●	0.3	0.7	1.4	µs
$t_{pG(EN,ON)}$	G1 to G3 Turn-On Delay From EN	V_{OUT} = 11V, Rising EN Edge to (G1 to G3) = (VS1 to VS3) – 3V, C_{GATE} = 10nF	●	1	1.4	2	µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. For all tests, V1 = VS1, V2 = VS2, V3 = VS3. Unless otherwise noted, V1 = V2 = V3 = V_{OUT} = 12V, HYS = GND.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input/Output Pins							
$V_{\overline{VALID}(OL)}$	$\overline{VALID1}$ to $\overline{VALID3}$ Output Low Voltage	I = 1mA, (V1 to V3) = 2.5V, V_{OUT} = 0V	●		0.25	0.55	V
$t_{p\overline{VALID}(OFF)}$	$\overline{VALID1}$ to $\overline{VALID3}$ Delay OFF From OV/UV Fault		●	5	8	13	µs
$V_{CAS(OH)}$	CAS Output High Voltage	I = –1µA	●	1.4	2	3	V
$V_{CAS(OL)}$	CAS Output Low Voltage	I = 1mA	●		0.2	0.4	V
I_{CAS}	CAS Pull-Up Current	$\overline{SHDN}$ = 0V, CAS = 1V	●	–6	–20	–40	µA
$t_{pCAS(EN)}$	CAS Delay from $V_{G(OFF)}$	V_{OUT} = 11V	●	0.4	0.7	1.3	µs
$V_{EN(THR)}$	EN Threshold Voltage	EN Rising	●	0.6	1	1.4	V
$V_{\overline{SHDN}(THR)}$	$\overline{SHDN}$ Threshold Voltage	$\overline{SHDN}$ Rising	●	0.4	0.8	1.2	V
$V_{\overline{SHDN}_EN(HYS)}$	$\overline{SHDN}$, EN Threshold Hysteresis				100		mV
$I_{\overline{SHDN}_EN}$	$\overline{SHDN}$, EN Pull-Up Current	$\overline{SHDN}$ = EN = 0V	●	–0.5	–2	–5	µA
I_{LEAK}	$\overline{SHDN}$, EN, $\overline{VALID1}$ to $\overline{VALID3}$, CAS Leakage Current	$\overline{SHDN}$ = EN = ($\overline{VALID1}$ to $\overline{VALID3}$) = 36V, CAS = 5.5V	●			±1	µA
OV, UV Protection Circuitry							
$V_{OV_UV(THR)}$	OV1 to OV3, UV1 to UV3 Comparator Threshold	V_{OUT} = 11V, OV1 to OV3 Rising, UV1 to UV3 Falling	●	0.985	1	1.015	V
$V_{OV_UV(HYS)}$	OV1 to OV3, UV1 to UV3 Comparator Hysteresis	V_{OUT} = 11V	●	15	30	45	mV
$I_{UV_OV(LEAK)}$	OV1 to OV3, UV1 to UV3 Leakage Current	OV1 to OV3 = 1.015V, UV1 to UV3 = 0.985V	●			±20	nA
$I_{OV_UV(MIN)}$	Minimum External Hysteresis Current	I_{HYS} = –400nA	●	35	50	75	nA
$I_{OV_UV(MAX)}$	Maximum External Hysteresis Current	I_{HYS} = –4µA	●	420	520	620	nA
V_{HYS}	HYS Voltage	I_{HYS} = –4µA	●	470	495	520	mV
$t_{\overline{VALID}}$	V1 to V3 Validation Time			100	256	412	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: Each V1 to V3 supply current specification includes current into the corresponding VS1 to VS3 for the channel(s) being tested.

Note 4: Specification represents the total diode-ORed current of V1 to V3 input supplies, selecting the highest voltage as the input source. If two input supplies are similar in voltage and higher than the remaining input supply voltage, the current is split evenly between the two higher voltage supplies. Current is split evenly if all supplies are equal.

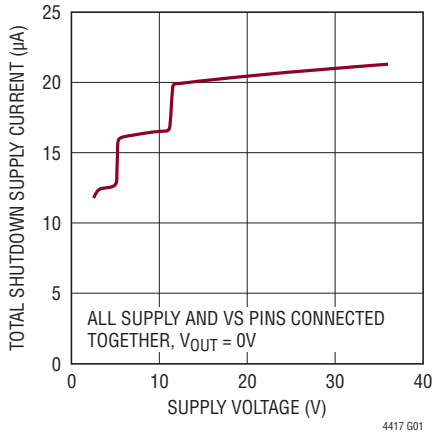
Note 5: Falling edge of G1 to G3 measured from 11V to 8V.

Note 6: Rising edge of G1 to G3 measured from 7V to 11V.

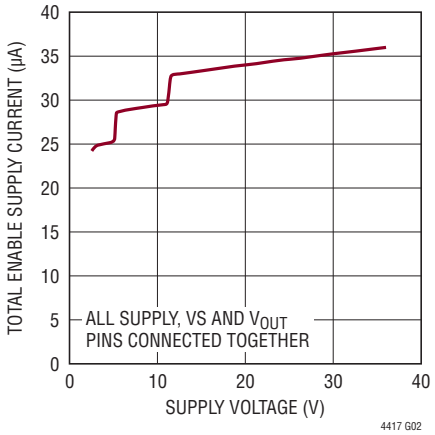
Note 7: UV1 driven below $V_{OV,UV(THR)}$. Time is measured from respective rising edge G1 to G3 crossing (VS1 to VS3) – 3V to next valid priority falling edge G1 to G3 crossing (VS1 to VS3) – 3V.

TYPICAL PERFORMANCE CHARACTERISTICS

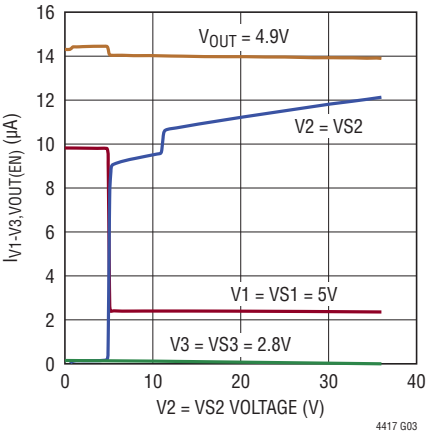
Total Shutdown Supply Current vs Supply Voltage



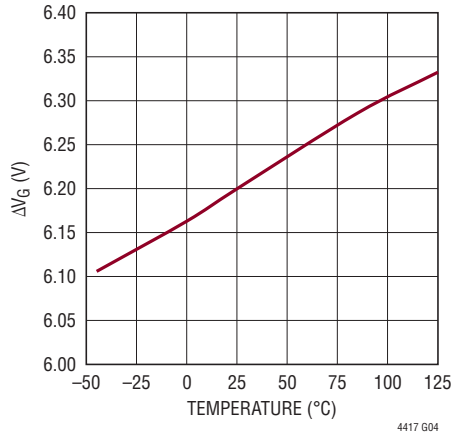
Total Enabled Supply Current vs Supply Voltage



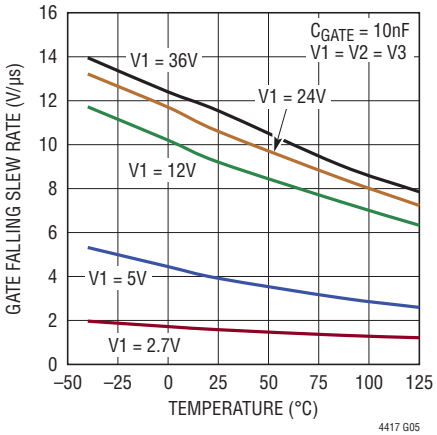
$I_{V1-V3,VOUT(EN)}$ vs Supply Voltage



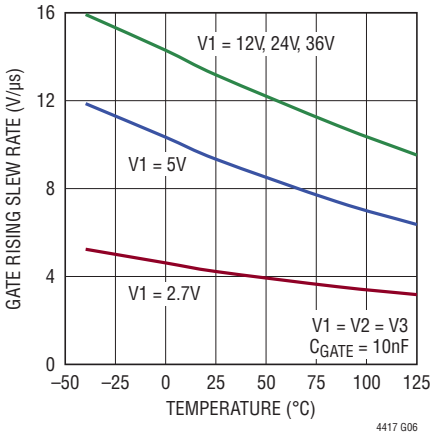
ΔV_G vs Temperature



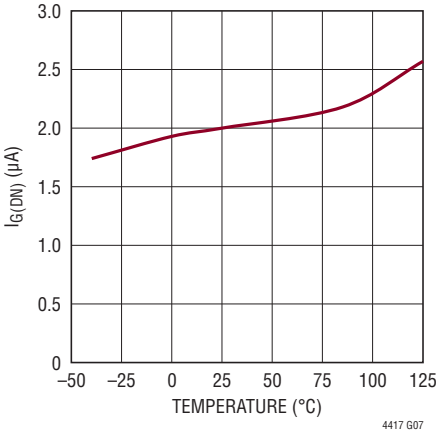
Gate Falling Slew Rate vs Temperature



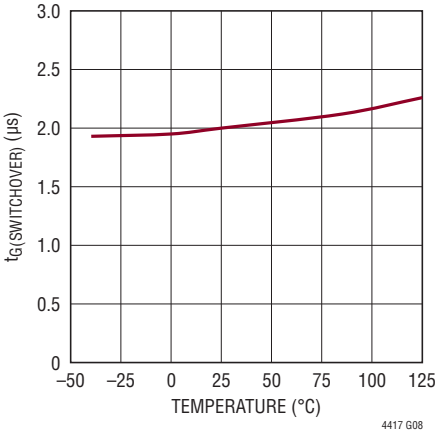
Gate Rising Slew Rate vs Temperature



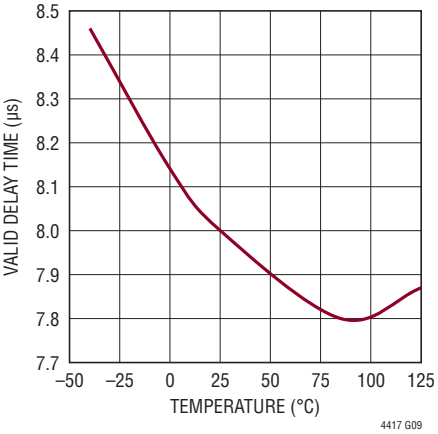
$I_{G(DN)}$ vs Temperature



Switchover Time vs Temperature

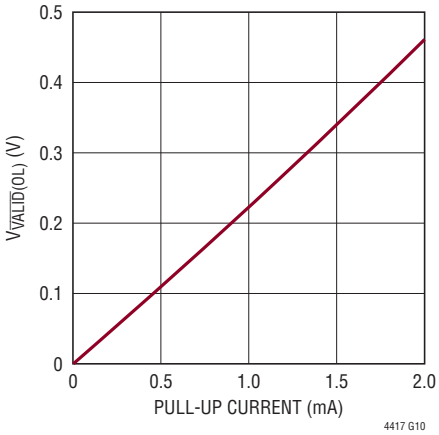


Valid Delay Off Time vs Temperature

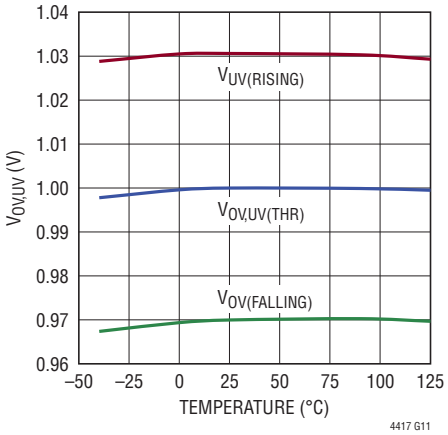


TYPICAL PERFORMANCE CHARACTERISTICS

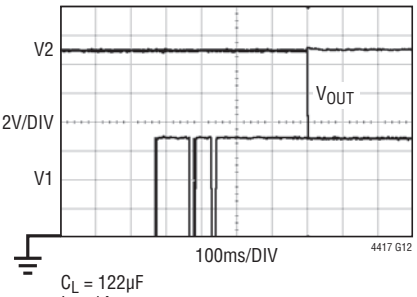
$V_{\overline{VALID}(OL)}$ vs Pull-Up Current



$V_{OV,UV}$ vs Temperature

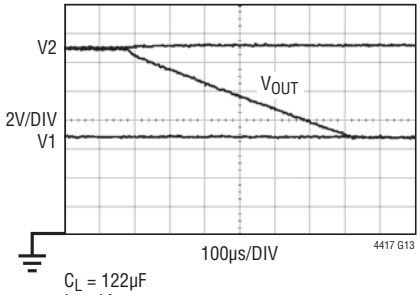


Deglitched Connection



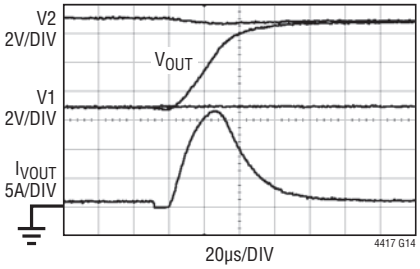
C_L = 122µF
I_L = 1A
–40V PCH FDD4685

V_{OUT} Switching from Higher to Lower Voltage



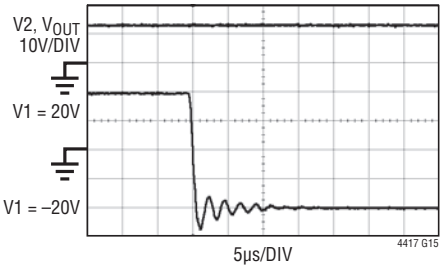
C_L = 122µF
I_L = 1A
–40V PCH FDD4685

V_{OUT} Switching from Lower to Higher Voltage with Slew Rate Control Circuitry



R_S = 1.43kΩ
C_S = 6.8nF
C_L = 100µF
I_L = 1A
–40V PCH FDD4685

Reverse Voltage Blocking



C_L = 122µF
I_L = 1A
–40V PCH FDD4685

PIN FUNCTIONS

CAS: Cascade Output. Digital output used for cascading multiple LTC4417s. Connect CAS to EN of another LTC4417 to increase the number of multiplexed input supplies. CAS is pulled up to the internal V_{LDO} voltage by an internal 20µA current source to indicate when all inputs are invalid, the external P-channel MOSFETs are determined to be off, and EN is above 1V. CAS also pulls high when $\overline{SHDN}$ is driven below 1V. CAS is pulled low when any input supply is within the OV/UV window for at least 256ms and both $\overline{SHDN}$ and EN are above 1V. CAS also pulls low when EN is driven below 1V. CAS can be driven to 5.5V independent of the input supply voltages. Leave open if not used.

EN: Channel Enable Input. EN is a high voltage input that allows the user to quickly connect and disconnect channels without resetting the OV/UV timers. When below 1V, all external back-to-back P-channel MOSFETs are driven off by pulling G1, G2 and G3 to their respective VS1, VS2 and VS3. When above 1V, the highest valid priority channel is connected to the output. EN is pulled to the internal V_{LDO} voltage with a 2µA current source and can be pulled up externally to a maximum voltage of 36V. Leave open when not used.

Exposed Pad (UF Package Only): Exposed pad may be left open or connected to device ground.

PIN FUNCTIONS

G1, G2, G3: P-Channel MOSFET Gate Drive Outputs. G1, G2 and G3 are used to control external back-to-back P-channel MOSFETs. When driven low, G1, G2 and G3 are clamped 6V below their corresponding VS1, VS2 and VS3. Connect G1, G2 and G3 to external P-channel MOSFET gate pins. See Dual Channel Applications Section for connecting unused channels.

GND: Device Ground.

HYS: OV/UV Comparator Hysteresis Input. Connecting HYS to ground sets a fixed 30mV hysteresis for the OV and UV comparators. Connecting a resistor, R_{HYS}, between HYS and ground disables the internal 30mV hysteresis and sets a 63mV/R_{HYS} hysteresis current which is sourced from each OV1, OV2 and OV3 and sunk into each UV1, UV2 and UV3 pin. Connect to ground when not used.

OV1, OV2, OV3: Overvoltage Comparator Inputs. Rising voltages above 1V signal an over voltage event, invalidating the respective input supply channel. Connect OV1, OV2 and OV3 to an external resistive divider from its respective V1, V2 and V3 to achieve the desired overvoltage threshold. The comparator hysteresis can be set to an internally fixed 30mV or set externally via the HYS pin. Connect unused pins to ground.

$\overline{\text{SHDN}}$: Shutdown Input. Driving $\overline{\text{SHDN}}$ below 0.8V turns off all external back-to-back P-channel MOSFET devices, forces the LTC4417 into a low current state, and resets the 256ms timers used to validate V1, V2 and V3. Driving $\overline{\text{SHDN}}$ above 0.8V allows channels to validate and connect. $\overline{\text{SHDN}}$ is pulled high to the internal V_{LDO} voltage with a 2µA current source and can be pulled up externally to a maximum voltage of 36V. Leave open when not used.

UV1, UV2, UV3: Undervoltage Comparator Inputs. Falling voltages below 1V signal an undervoltage event, invalidating the respective input supply channel. Connect UV1, UV2 and UV3 through a resistive divider between the respective V1, V2 and V3 and ground to achieve the desired undervoltage threshold. The comparator hysteresis can be set to an internally fixed 30mV or set externally via the HYS pin. Connect pins from unused channels to ground.

V1: Highest Priority Input Supply. When V1 is within its user defined OV/UV window for 256ms, it is connected to V_{OUT} via its external back-to-back P-channel MOSFETs. Connect V1 to ground when channel is not used. See Applications Information for bypass capacitor recommendations.

V2: Second Priority Input Supply. When V2 is within its OV/UV window for 256ms, it is connected to V_{OUT} via its external back-to-back P-channel MOSFETs only if V1 does not meet its OV/UV requirements. Connect to ground when channel is not used. See Applications Information for bypass capacitor recommendations.

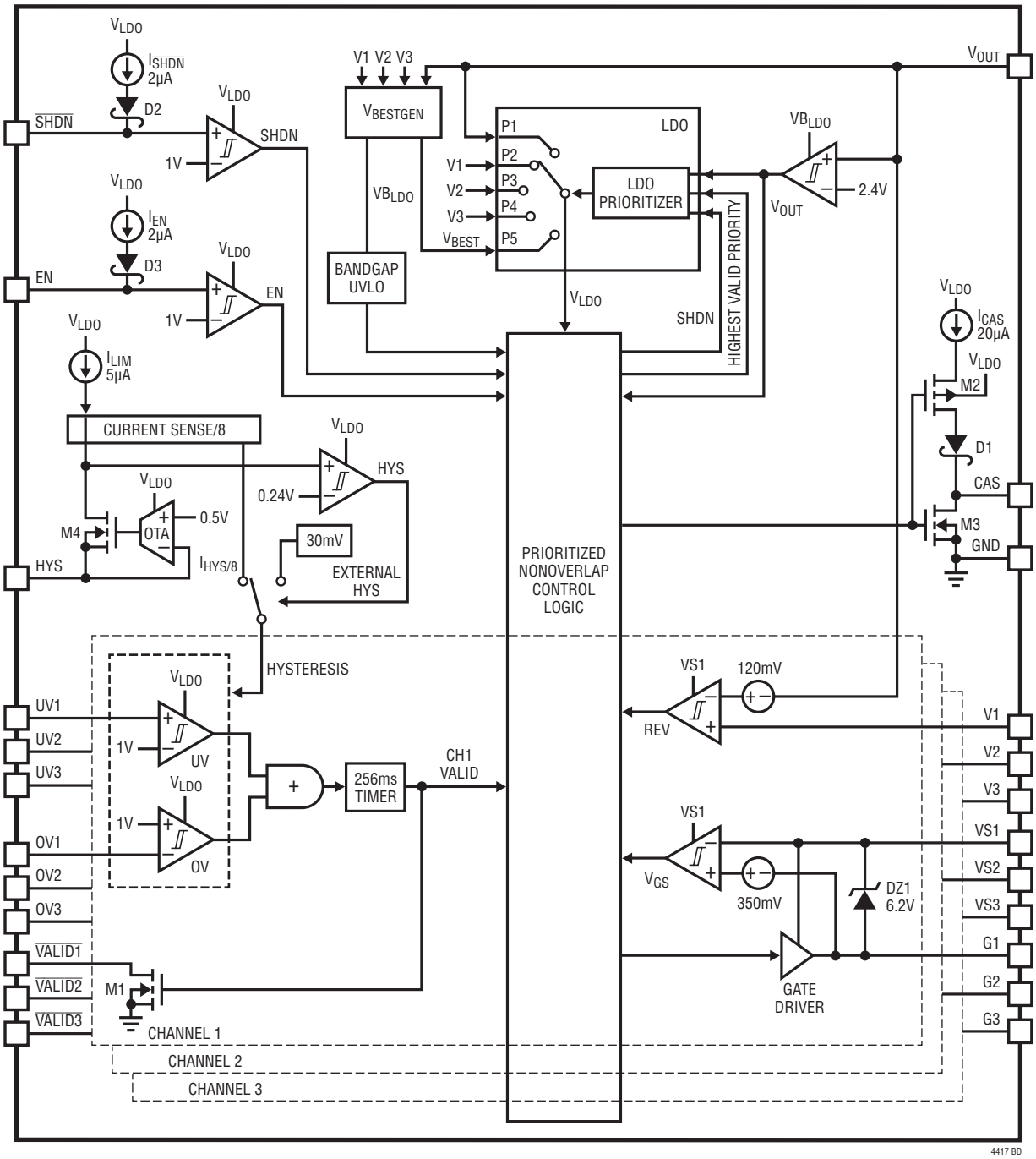
V3: Third Priority Input Supply. When V3 is within its OV/UV window for 256ms, it is connected to V_{OUT} via its external back-to-back P-channel MOSFETs only if V1 and V2 do not meet their OV/UV requirements. Connect to ground when channel is not used. See Applications Information for bypass capacitor recommendations.

$\overline{\text{VALID1}}$, $\overline{\text{VALID2}}$, $\overline{\text{VALID3}}$: Valid Channel Indicator Outputs. $\overline{\text{VALID1}}$, $\overline{\text{VALID2}}$ and $\overline{\text{VALID3}}$ are high voltage open drain outputs that pull low when the respective V1, V2 and V3 are within the OV/UV window for at least 256ms and release when the respective V1, V2 and V3 are outside the OV/UV window. Connect a resistor between $\overline{\text{VALID1}}$, $\overline{\text{VALID2}}$ and $\overline{\text{VALID3}}$ and a desired supply, up to a maximum of 36V, to provide the pull-up. Leave open when not used.

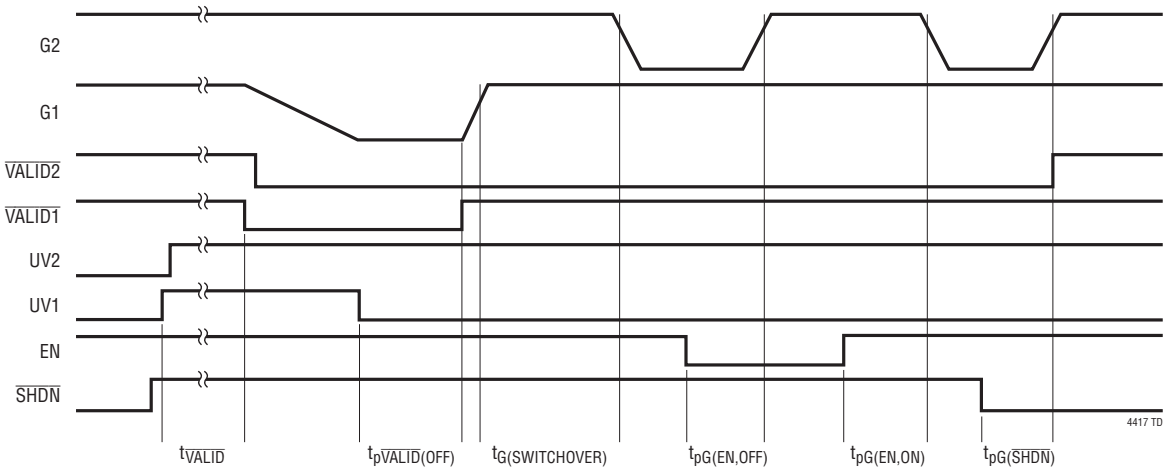
VS1, VS2, VS3: External P-Channel MOSFET Common Source Connection. VS1, VS2 and VS3 supply the higher voltage of V1, V2 and V3 or V_{OUT} to the gate drivers. Connect VS1, VS2 and VS3 to the respective common source connection of the back-to-back P-channel MOSFETs. Connect to ground when channel is not used. See Applications Information section for bypass capacitor recommendations.

V_{OUT}: Output Voltage Supply and Sense. V_{OUT} is an output voltage sense pin used to prevent any input supply from connecting to the output if the output voltage is not at least 120mV below the input supply voltage. During normal operation, V_{OUT} powers most of the internal circuitry when its voltage exceeds 2.4V. Connect V_{OUT} to the output. See Applications Information section for bypass capacitor recommendations.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

The Functional Block Diagram displays the main functional blocks of this device. The LTC4417 connects one of three power supplies to a common output, V_{OUT}, based on user defined priority. Connection is made by enhancing external back-to-back P-channel MOSFETs. Unlike a diode-OR, which always passes the highest supply voltage to the output, the LTC4417 lets one use a lower voltage supply for primary power and a higher voltage supply as secondary or backup power.

During normal operation the LTC4417 continuously monitors V1, V2 and V3 through its respective OV1, OV2 and OV3 and UV1, UV2 and UV3 pins using precision overvoltage and undervoltage comparators. The highest priority input supply whose voltage is within its respective OV/UV window for at least 256ms is considered valid and is connected to V_{OUT} through external back-to-back P-channel MOSFETs. $\overline{VALID1}$, $\overline{VALID2}$ and $\overline{VALID3}$ pull low to indicate when the V1, V2 and V3 input supplies are valid.

Hysteresis on the OV and UV threshold is adjustable. Connecting a resistor, R_{HYS}, between HYS and ground forces 63mV/R_{HYS} current to flow out of OV1, OV2 and OV3 and into UV1, UV2 and UV3 to create hysteresis when outside their respective OV/UV windows. Connecting HYS to ground sets the OV and UV comparator hysteresis to 30mV. See the Application Information for more details.

During channel transitions, monitoring circuitry prevents cross conduction between input channels and reverse conduction from V_{OUT} using a break-before-make architecture. The VGS comparator monitors the disconnecting channel's gate pin voltage (G1, G2 or G3). When the gate voltage is 350mV from its common source connection (VS1, VS2 or VS3), the VGS comparator latches the output to indicate the channel is off and allows the next valid priority input supply to connect to V_{OUT}, preventing cross conduction between channels. The latch is reset when the channel is turned on.

To prevent reverse conduction from V_{OUT} to V1, V2 and V3 during channel switchover, the REV comparator monitors the connecting input supply (V1, V2 or V3) and output voltage (V_{OUT}). The REV comparator delays the connection until the output voltage droops lower than the input voltage by the reverse current blocking threshold of 120mV. The output of the REV comparator is latched, resetting when its respective channel is turned off.

The LTC4417 gate driver pulls down on G1, G2 and G3 with a strong P-channel source follower and a 2µA current source. When the clamp voltage is reached, the P-channel source follower is back biased, leaving the 2µA current source to hold G1, G2 and G3 at the clamp voltage. To minimize inrush current at start-up, the gate driver soft-starts the first input supply to connect V_{OUT}, at a rate of around 5V/ms terminating when any channel disconnects or 32ms has elapsed. Once slew rate control has terminated, the gate driver quickly turns on and off external back-to-back P-channel MOSFETs as needed. A $\overline{SHDN}$ low to high transition or V_{OUT} drooping below 0.7V reactivates soft-start.

When EN is driven above 1V the highest valid priority input supply is connected to V_{OUT}. The high voltage EN comparator disconnects all channels when EN is driven below 1V. The LTC4417 continues to monitor the OV and UV pins and reflects the current input supply status with $\overline{VALID1}$, $\overline{VALID2}$ and $\overline{VALID3}$. When four or more supplies need to be prioritized, connect the higher priority LTC4417's CAS to the lower priority LTC4417's EN. If V_{OUT} is allowed to fall below 0.7V, the next connecting input supply is soft-started.

The high voltage $\overline{SHDN}$ comparator forces the LTC4417 into a low current state when $\overline{SHDN}$ is forced below 0.8V. While in the low current state, all channels are disconnected, OV and UV comparators are disabled, and all 256ms timers are reset. When $\overline{SHDN}$ transitions from low to high, the first validated input to connect to V_{OUT} is soft-started.

Two separate internal power rails ensure the LTC4417 is functional when one or more input supply is present and above 2.3V. $V_{BESTGEN}$ generates a VB_{LDO} rail from the highest V1, V2 and V3 and V_{OUT} voltage. VB_{LDO} powers the UVLO, bandgap, and V_{OUT} comparator. The internal V_{LDO} powers all other circuits from V_{OUT} provided V_{OUT} is greater than 2.4V. If V_{OUT} is less than 2.3V, V_{LDO} powers all other circuits from the highest priority supply available. If all sources are invalid or the LTC4417 is shut down, V_{LDO} connects to VB_{LDO}.

APPLICATIONS INFORMATION

INTRODUCTION

The LTC4417 is an intelligent high voltage triple load switch which automatically connects one of three input supplies to a common output based on predefined pin priorities and validity. V1 is defined to be the highest priority and V3 the lowest priority, regardless of voltage. An input supply is defined valid when the voltage remains in the user defined overvoltage (OV) and undervoltage (UV) window for at least 256ms.

If a connected input supply falls out of the user defined OV/UV window and remains outside the OV/UV window for at least 8µs, the channel is disconnected and the next highest valid priority is connected to the common output. If a lower priority input supply is connected to V_{OUT} and a higher priority input supply becomes valid, the LTC4417 disconnects the lower priority supply and connects the higher priority input supply to V_{OUT}.

Typical LTC4417 applications are systems where predictable autonomous load control of multiple input supplies is desired. These supplies may not necessarily be different in voltage, nor must the highest voltage be the primary supply. A typical LTC4417 application circuit is shown in Figure 1. External component selection is discussed in detail in the following sections.

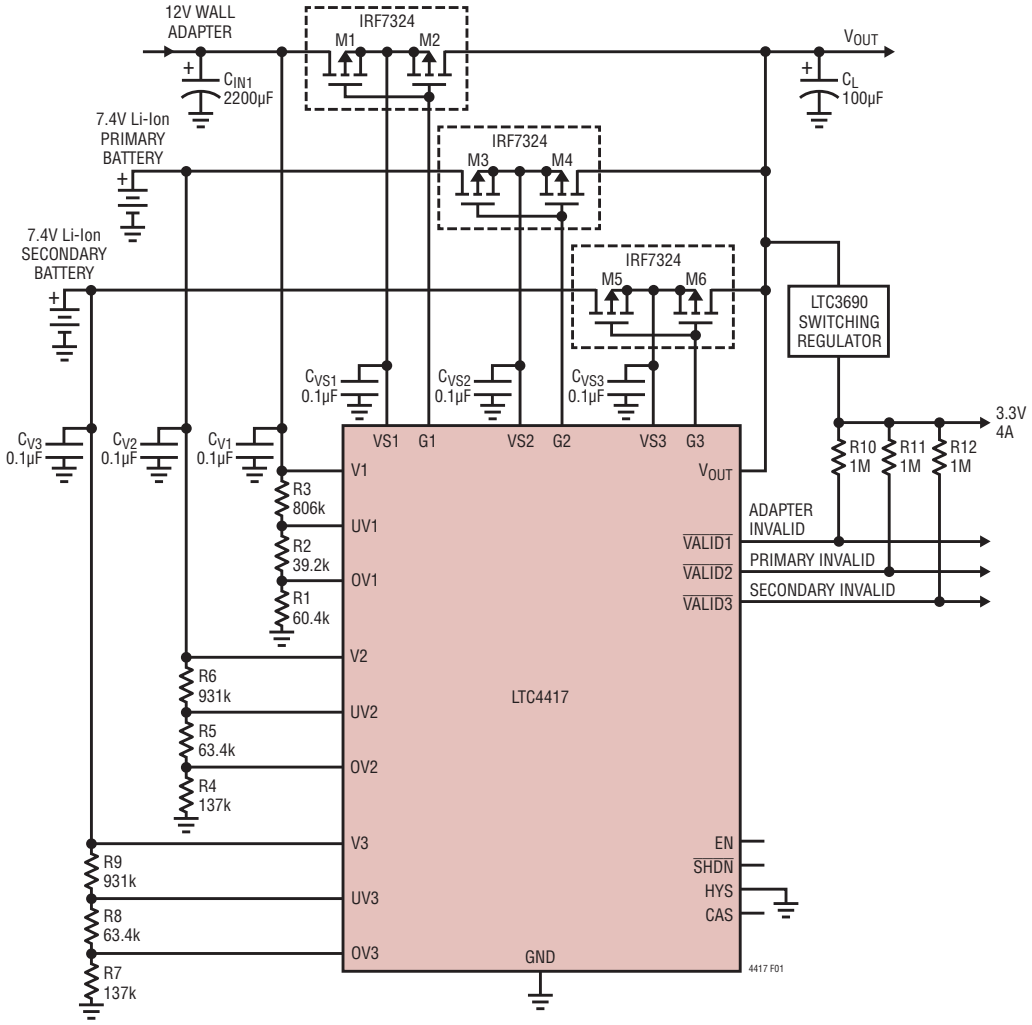


Figure 1. Typical Hand Held Computer Application.

APPLICATIONS INFORMATION

DEFINING OPERATIONAL RANGE

To guard against noise and transient voltage events during live insertion, the LTC4417 requires an input supply remain in the OV/UV window for at least 256ms to be valid. The OV/UV window for each input supply is set by a resistive divider (for example, R1, R2 and R3 for V1 input supply) connected from the input supply to GND, as shown in Figure 1. When setting the resistive divider values for the OV and UV input supply threshold, take into consideration the tolerance of the input supply, 1.5% error in the OV and UV comparators, tolerance of R1, R2 and R3, and the ±20nA maximum OV/UV pin leakage currents.

In addition to tolerance considerations, hysteresis reduces the valid input supply operating range. Input supplies will need to be within the reduced input supply operating range to validate. Referring to Figure 2, V1 supply voltage must be greater than UV_{HYS} to exit the UV fault. If an OV fault occurs, the V1 supply voltage must return to a voltage lower than the OV_{HYS} voltage to exit the OV fault.

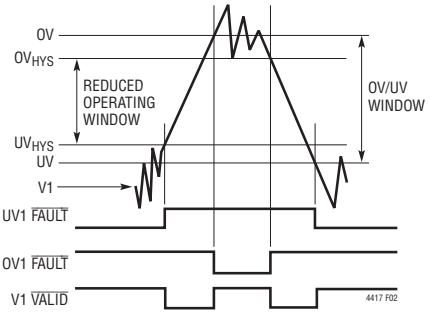


Figure 2. OV and UV Thresholds and Hysteresis Voltage

Hysteresis for the OV and UV comparators are set via the HYS pin. Two options are available. Connecting a resistor, R_{HYS}, between HYS and GND, as shown in Figure 3, sets the hysteresis current $I_{OV_UV(HYS)}$ that is sunk into UV1, UV2 and UV3 and sourced out of OV1, OV2 and OV3. The value of R_{HYS} is calculated with Equation (1). Choose R_{HYS} to limit the hysteresis current to between 50nA and 500nA.

$$R_{HYS} = \frac{63mV}{I_{OVUV(HYS)}} \quad (1)$$

where $50nA \le I_{OVUV(HYS)} \le 500nA$

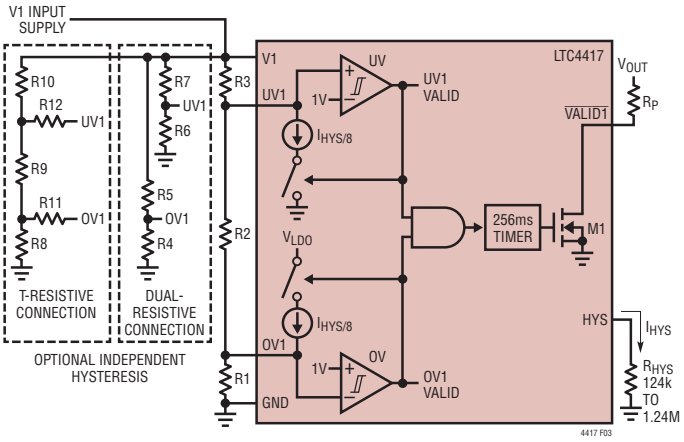


Figure 3. LTC4417 External Hysteresis

Independent OV and UV hysteresis values are available by separating the single string resistive dividers R1, R2 and R3, shown in Figure 3, into two resistive strings, R4-R5 and R6-R7. In such a configuration, the top resistor defines the amount of hysteresis and the bottom resistor defines the threshold. Use Equations (2) and (3) to calculate the values.

$$R_{TOP} = \frac{HYST}{I_{OVUV(HYS)}} \quad (2)$$

where HYST is the desired hysteresis voltage at V1.

$$R_{BOTTOM} = \frac{R_{TOP}}{(OV/UV\,Threshold) - 1} \quad (3)$$

When large independent hysteresis voltages are required, a resistive T structure can be used to define hysteresis values, also shown in Figure 3. After the desired OV and UV thresholds are set with resistors R8 through R10, R11 and R12 are calculated using:

$$R11 = \frac{R8 \bullet \left[OV_{HYS} - I_{OVUV(HYS)} \bullet (R9 + R10)\right]}{I_{OVUV(HYS)} \bullet (R8 + R9 + R10)} \quad (4)$$

$$R12 = \frac{(R8 + R9) \bullet \left[UV_{HYS} - I_{OVUV(HYS)} \bullet R10\right]}{I_{OVUV(HYS)} \bullet (R8 + R9 + R10)} \quad (5)$$

where OV_{HYS}, UV_{HYS} are the desired OV and UV hysteresis voltage magnitudes at V1 through V3, and $I_{OVUV(HYS)}$ is the programmed hysteresis current.

APPLICATIONS INFORMATION

Reduction of the valid operating range can be used to prevent disconnected high impedance input supplies from reconnecting. For example, if 3 series connected AA Alkaline batteries with a total series resistance of 675mΩ is used to source 500mA, the voltage drop due to the series resistance would be 337.5mV. Once the batteries are discharged and are disconnected due to a UV fault, the AA battery stack would recover the 337.5mV drop across the internal series resistance. Using the 30mV fixed internal hysteresis allows only 81mV of hysteresis at the input pin, possibly allowing the input supply to revalidate and reconnect. Using external hysteresis, the hysteresis voltage can be increased to 400mV, reducing or eliminating the reconnection issue, as shown in Figure 4.

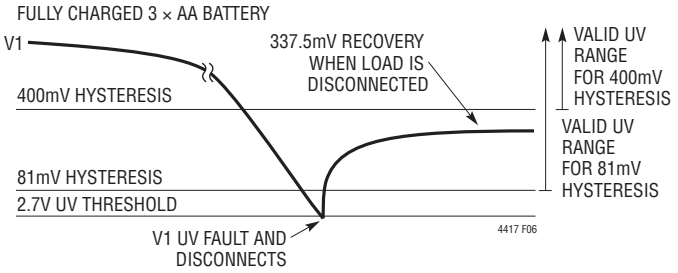


Figure 4. Setting a Higher UV Hysteresis to Prevent Unwanted Reconnections

Connecting HYS to GND, as shown in Figure 5, selects an internal 30mV fixed hysteresis, resulting in 3% of the input supply voltage.

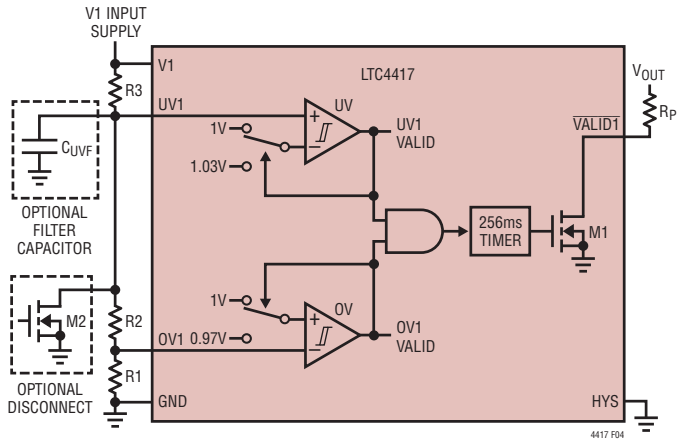


Figure 5. LTC4417 Internal Hysteresis with Optional Filter Capacitor and Manual Disconnect MOSFET

FILTERING NOISE ON OV AND UV PINS

The LTC4417 provides an 8µs OV/UV fault filter time. If the 8µs filter time is not sufficient, add a filter capacitor between the OV or UV pin and GND to extend the fault filter time and ride through transient events. A UV pin fault filter time extension capacitor, C_{UVF}, is shown in Figure 5.

Use Equation (6) to select C_{UVF} for the UV pin and Equation (7) to select C_{OVF} for the OV pin.

$$C_{UVF} = t_{DELAY} \bullet \frac{R1+R2+R3}{R3 \bullet (R1+R2)} \bullet \ln\left[\frac{V_i - V_f}{1V - V_f}\right] \quad (6)$$

$$C_{OVF} = t_{DELAY} \bullet \frac{R1+R2+R3}{R1 \bullet (R2+R3)} \bullet \ln\left[\frac{V_i - V_f}{1V - V_f}\right] \quad (7)$$

where the final input voltage V_f and the initial voltage V_i are the resistively divided down values of the input supply step, as shown in Figure 6.

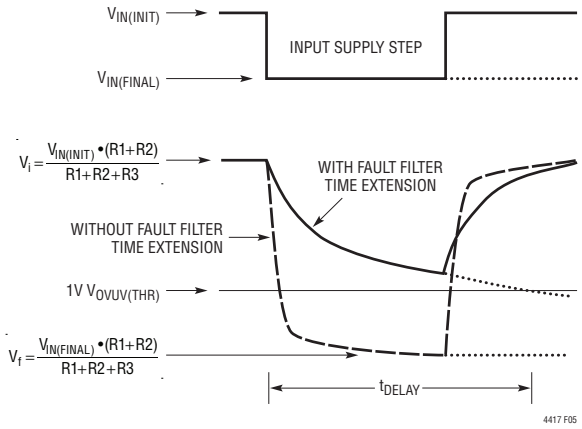


Figure 6. Fault Filter Time Extension

Extending the filter time delay will result in a slower response to fast UV and OV faults. Extending the UV pin fault filter time delay will also add delay to the OV pin. If this is not desirable, separate the single resistive string into two resistive strings, as shown in Figure 3.

PRIORITY REASSIGNMENT

A connected input supply can be manually disconnected by artificially creating a UV fault. An example is shown in Figure 5. When N-channel MOSFET, M2, is turned on, the

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UV1 pin is pulled below 1V. The LTC4417 then disconnects V1 and connects the next highest valid priority to V_{OUT}. When selecting the external N-channel MOSFET, be sure to account for drain leakage current when setting UV and OV thresholds by adjusting the resistive divider to consume more current.

SELECTING EXTERNAL P-CHANNEL MOSFETS

The LTC4417 drives external back-to-back P-channel MOSFETs to conduct or block load current between an input supply and load. When selecting external P-channel MOSFETs, the key parameters to consider are on-resistance ($R_{DS(ON)}$), absolute maximum rated drain to source breakdown voltage ($BV_{DSS(MAX)}$), threshold voltage ($V_{GS(TH)}$), power dissipation, and safe operating area (SOA).

To determine the required $R_{DS(ON)}$ use Equation (8), where V_{DROP} is the maximum desired voltage drop across the two series MOSFETs at full load current, $I_{L(MAX)}$, for the application. External P-channel MOSFET devices may be paralleled to further decrease resistance and decrease power dissipation of each paralleled MOSFET.

$$R_{DS(ON)} \leq \frac{V_{DROP}}{2 \bullet I_{L(MAX)}} \quad (8)$$

The clamped gate drive output is 4.5V (minimum) from the common source connection. Select logic level or lower threshold external MOSFETs to ensure adequate overdrive. For applications with input supplies lower than the clamp voltage, choose external MOSFET with thresholds sufficiently lower than the input supply voltage to guarantee full enhancement.

It is imperative that external P-channel MOSFET devices never exceed their $BV_{DSS(MAX)}$ rating in the application. Select devices with $BV_{DSS(MAX)}$ ratings higher than seen in the application. Switching inductive supply inputs with low value input and/or output capacitances may require additional precautions; see Transient Supply Protection section in this data sheet for more information.

In normal operation, the external P-channel MOSFET devices are either fully on, dissipating relatively low power, or off, dissipating no power. However, during slew-rate controlled start-up, significant power is dissipated in the external P-channel MOSFETs. The external P-channel MOSFETs dissipate the maximum amount of power during the initial slew-rate limited turn on, where the full input voltage is applied across the MOSFET while it sources current. Power dissipation immediately starts to decrease as the output voltage rises, decreasing the voltage drop across the MOSFETs.

A conservative approach for determining if a particular device is capable of supporting soft-start, is to ensure its maximum instantaneous power, at the start of the output slewing, is within the manufacturer's SOA curve. First determine the duration of soft-start using Equation (9) and find the inrush current into the load capacitor using Equation (10).

$$t_{STARTUP} = \frac{V_{IN}}{5[V/ms]} \quad (9)$$

$$I_{MAXCAP} = C_L \bullet 5000[V/s] \quad (10)$$

Using V_{IN} and I_{MAXCAP}, the power dissipated by the external MOSFETs during start-up, P_{SS}, is defined by Equation (11). If the LTC4417 soft-starts with a live I_L, the extra load current needs to be added to I_{MAXCAP}, and P_{SS} is calculated by Equation (12).

$$P_{SS} = V_{IN} \bullet I_{MAXCAP} \quad (11)$$

$$P_{SS} = V_{IN} \bullet (I_{MAXCAP} + I_L) \quad (12)$$

Check to ensure P_{SS} with a $t_{STARTUP}$ single pulse duration lies within the safe operating area (SOA) of the chosen MOSFET. Ensure the resistive dividers can sink the drain-source leakage current at the maximum operating temperature. Refer to manufacturer's data sheet for maximum drain to source leakage currents, I_{DSS}.

A list of suggested P-channel MOSFETs is shown in Table 1. Use procedures outlined in this section and the SOA curves in the chosen MOSFET manufacturer's data sheet to verify suitability for the application.

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Table 1. List of Suggested P-Channel MOSFETs

V1, V2, V3	MOSFET	$V_{TH(MAX)}$	$V_{GS(MAX)}$	$V_{DS(MAX)}$	MAX RATED $R_{DS(ON)}$ AT 25°C
≤5V	Si4465ADY	–1V	±8V	–8V	9mΩ at –4.5V 11mΩ at –2.5V
≤10V	Si4931DY*	–1V	±8V	–12V	18mΩ at –4.5V 22mΩ at –2.5V
≤18V	FDS8433A	–1V	±8V	–20V	47mΩ at –4.5V 70mΩ at –2.5V
≤18V	IRF7324*	–1V	±12V	–20V	18mΩ at –4.5V 26mΩ at –2.5V
≤28V	Si7135DP	–3V	±20V	–30V	6.2mΩ at –4.5V
≤28V	FDS6675BNZ	–3V	±20V	–30V	22mΩ at –4.5V
≤28V	AO4803A*	–2.5V	±20V	–30V	46mΩ at –4.5V
≤36V	SUD50P04	–2.5V	±20V	–40V	30mΩ at –4.5V
≤36V	FDD4685	–3V	±20V	–40V	35mΩ at –4.5V
≤36V	FDS4685	–3V	±20V	–40V	35mΩ at –4.5V
≤36V	Si4909DY*	–2.5V	±20V	–40V	34mΩ at –4.5V
≤36V	Si7489DP	–3V	±20V	–100V	47mΩ at –4.5V

*Denotes Dual P-Channel

REVERSE VOLTAGE PROTECTION

The LTC4417 is designed to withstand reverse voltages applied to V1, V2 and V3 with respect to V_{OUT} of up to –84V. The large reverse voltage rating protects 36V input supplies and downstream devices connected to V_{OUT} against high reverse voltage connections of –42V (absolute maximum) with margin.

Select back-to-back P-channel MOSFETS with $BV_{DSS(MAX)}$ ratings capable of handling any anticipated reverse voltages between V_{OUT} and V1, V2 or V3. Ensure transient voltage suppressors (TVS) connected to reverse connection protected inputs (V1, V2 and V3) are bidirectional and input capacitors are rated for the negative voltage.

REVERSE CURRENT BLOCKING

When switching channels from higher voltages to lower voltages, the REV comparator verifies the V_{OUT} voltage is below the connecting channel's voltage by 120mV before the new channel is allowed to connect to V_{OUT}. This ensures little to no reverse conduction occurs during switching.

An example is shown in Figure 7. V2 is initially connected to V_{OUT} when a higher priority input supply, V1, is inserted.

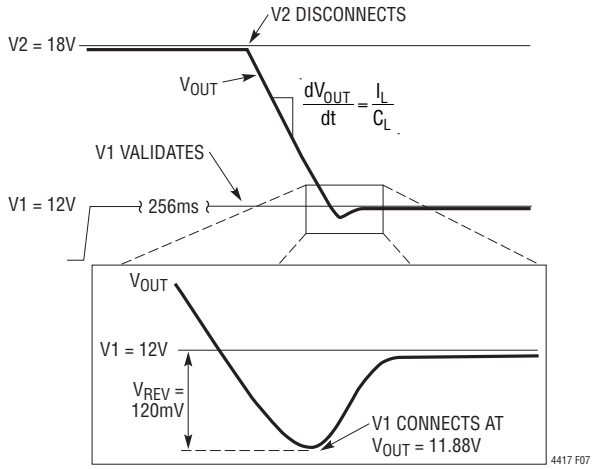


Figure 7. Reverse Current Blocking

The LTC4417 validates V1 and disconnects V2, allowing V_{OUT} to decay from 18V to 11.88V at a slew rate determined by the load current divided by the load capacitance. Once V_{OUT} falls to 11.88V, the LTC4417 connects V1 to V_{OUT}.

SELECTING V_{OUT} CAPACITANCE

To ensure there is minimal droop at the output, select a low ESR capacitor large enough to ride through the dead time between channel switchover. A low ESR bulk capacitor will reduce IR drops to the output voltage while the load current is sourced from the capacitor. Use Equation (13) to calculate the load capacitor value that will ride through the OV/UV comparator delay, $t_{p\overline{VALID}(OFF)}$, plus the break-before-make time, $t_{G(SWITCHOVER)}$.

$$C_L \geq \frac{I_{L(MAX)} \bullet \left(t_{G(SWITCHOVER)} + t_{p\overline{VALID}(OFF)}\right)}{V_{OUT_DROOP(MAX)}} \quad (13)$$

where $I_{L(MAX)}$ is the maximum load current drawn and $V_{OUT_DROOP(MAX)}$ is the maximum acceptable amount of voltage droop at the output.

Equation (13) assumes no inrush current limiting circuitry is required. If it is required, refer to Figure 8 and use the following Equation (14) for C_L.

$$C_L \geq \frac{I_{L(MAX)} \bullet \left(t_{G(SWITCHOVER)} + t_{p\overline{VALID}(OFF)} + 0.79 \bullet R_S \bullet C_S\right)}{V_{OUT_DROOP(MAX)}} \quad (14)$$

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where R_S and C_S are component values shown in Figure 8. The selection of R_S and C_L involves an iterative process. Begin by assuming 0.79 • R_S • C_S = 10µs and choosing C_L using Equation (14). See the Inrush Current and Input Voltage Droop section for more details regarding inrush current limiting circuitry, and for selecting R_S.

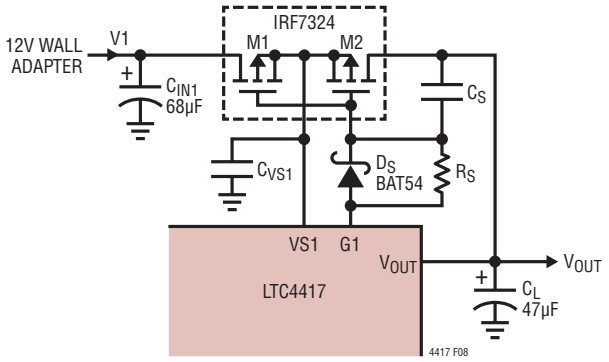


Figure 8. Slew Rate Limiting Gate Drive

GATE DRIVER

When turning a channel on, the LTC4417 pulls the common gate connection (G1, G2 and G3) down with a P-channel source follower and a 2µA current source. VS1, VS2 and VS3 voltages at or above 5V will produce rising slew rates of 12V/µs and falling slew rates of 4V/µs with 10nF between the VS and G pins. VS1, VS2 and VS3 voltages lower than 5V will result in lower slew rates, see typical curves for more detail. As G1, G2 and G3 approaches the 6.2V clamp voltage, the source follower smoothly reduces its current while the 2µA hold current continues to pull G1, G2 and G3 to the final clamp voltage, back biasing the source follower. Clamping the G1, G2 and G3 voltage prevents any overvoltage stress on the gate to source oxide of the external back-to-back P-channel MOSFETs. If leakage into G1, G2 and G3 exceeds the 2µA hold current, the G1, G2 and G3 voltage will rise above the clamp voltage, where the source follower enhances to sink the excess current. When turning a channel off, the gate driver pulls the common gate to the common source with a switch having an on-resistance of 16Ω, to effect a quick turn-off.

To minimize inrush current at start-up, the gate driver soft-starts the gate drive of the first input to connect to V_{OUT}. The gate pin is regulated to create a constant 5V/ms rise rate on V_{OUT}. Slew rate control is terminated when any channel disconnects or 32ms has elapsed. Once soft-start has terminated, the gate driver quickly turns on and off external back-to-back P-channel MOSFETs as needed. A $\overline{SHDN}$ low to high transition or V_{OUT} drooping below 0.7V reactivates soft-start.

INRUSH CURRENT AND INPUT VOLTAGE DROOP

When switching control of V_{OUT} from a lower voltage supply to a higher voltage supply, the higher voltage supply may experience significant voltage droop due to high inrush current during a fast connection to a lower voltage output bulk capacitor with low ESR. This high inrush current may be sufficient to trigger an undesirable UV Fault.

To prevent a UV fault when connecting a higher voltage input to a lower voltage output, without adding any inrush current limiting, size the input bypass capacitor large enough to provide the required inrush current, as shown by Equation (15).

$$C_{V1} \geq C_L \bullet \left(\frac{V1 - V_{OUT(INIT)}}{V1_{DROOP}} - 1 \right) \quad (15)$$

where $V_{OUT(INIT)}$ is the initial output voltage when being powered from a supply voltage less than V1, C_{V1} is the bypass capacitor connected to V1, C_L is the output capacitor and $V1_{DROOP}$ is the maximum allowed voltage droop on V1. Make sure C_{V1} is a low ESR capacitor to minimize the voltage step across the ESR.

In situations where input and output capacitances cannot be chosen to set the desired maximum input voltage droop, or the peak inrush current violates the maximum Pulsed Drain Current (I_{DM}) of the external P-channel MOSFETs, inrush current can be limited by slew rate limiting the output voltage. The gate driver can be configured to slew rate limit the output with a resistor, capacitor and Schottky diode, as shown in Figure 8. The series resistor R_S and capacitor, C_S, slew rate limit the output, while the Schottky diode, D_S, provides a fast turn off path when G1 is pulled to VS1.

With a desired input voltage drop, $V1_{DROOP}$, and known supply resistance R_{SRC}, the series resistance, R_S, can be calculated with Equation (16), where $\Delta V_{G(SINK)}$ is the LTC4417's sink clamp voltage, V_{GS} is the external

APPLICATIONS INFORMATION

P-channel's gate to source voltage when driving the load and inrush current, C_S is the slew rate capacitor and C_L is the V_{OUT} hold up capacitance. The output load current I_L is neglected for simplicity. Choose C_S to be at least ten times the external P-channel MOSFET's $C_{RSS(MAX)}$, and C_{VS} to be ten times C_S.

$$R_S \geq \frac{\left(\Delta V_{G(SINK)} - V_{GS}\right) \bullet C_L \bullet R_{SRC}}{C_S \bullet V1_{DROOP}} \quad (16)$$

Use Equation (17) to verify the inrush current limit is lower than the absolute maximum pulsed drain current, I_{DM}.

$$I_{INRUSH} = \frac{V1_{DROOP}}{R_{SRC}} \quad (17)$$

If the external P-channel MOSFET's reverse transfer capacitance, C_{RSS}, is used instead of C_S, replace C_S with C_{RSS} in Equation (16), where C_{RSS} is taken at the minimum V_{DS} voltage, and calculate for R_S. Depending on the size of C_{RSS}, R_S may be large. Care should be used to ensure gate leakages do not inadvertently turn off the channel over temperature. This is particularly true of built in Zener gate-source protected devices. Careful bench characterization is strongly recommended, as C_{RSS} is non-linear.

The preceding analysis assumes a small input inductance between the input supply voltage and the drain of the external P-channel MOSFET. If the input inductance is large, choose C_{V1} to be much greater than C_L and replace R_{SRC} with the ESR of C_{V1}.

When slew rate limiting the output, ensure power dissipation does not exceed the manufacturer's SOA for the chosen external P-channel MOSFET. Refer to the Selecting External P-channel MOSFETs section.

TRANSIENT SUPPLY PROTECTION

The LTC4417's abrupt switching due to OV or UV faults can create large transient overvoltage events with inductive input supplies, such as supplies connected by a long cable. At times the transient overvoltage condition can exceed twice the nominal voltage. Such events can damage external devices and the LTC4417. It is imperative that external back-to-back P-channel MOSFET devices do not exceed their single pulse avalanche energy specification (EAS) in unclamped inductive applications and input voltages to the LTC4417 never exceed the Absolute Maximum Ratings.

To minimize inductive voltage spikes, use wider and/or heavier trace plating. Adding a snubber circuit will dampen input voltage spikes as discussed in Linear Application Note 88, and a transient surge suppressor at the input will clamp the voltage. Transient voltage suppressors (TVS) should be placed on any input supply pin, V1, V2 and V3, where input shorts, or reverse voltage connection can be made. If short-circuit of input sources powering V_{OUT} are possible, transient voltage suppressors should also be placed on V_{OUT}, as shown in Figure 9.

When selecting transient voltage suppressors, ensure the reverse standoff voltage (V_R) is equal to or greater than the application operating voltage, the peak pulse current (I_{PP}) is higher than the peak transient voltage divided by the source impedance, the maximum clamping voltage (V_{CLAMP}) at the rated I_{PP} is less than the absolute maximum ratings of the LTC4417 and BV_{DSS} of all the external back-to-back P-channel MOSFETs.

In applications below 20V, transient voltage suppressors may not be required if the voltage spikes are lower than the BV_{DSS} of the external P-channel MOSFETs and the LTC4417

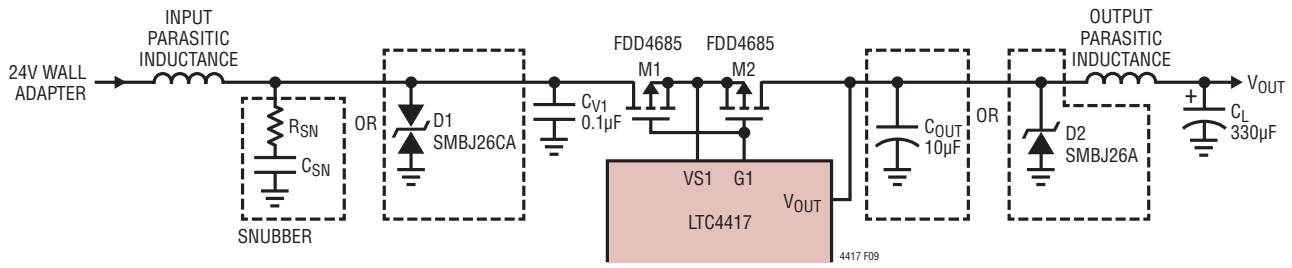


Figure 9. Transient Voltage Suppression

APPLICATIONS INFORMATION

Absolute Maximum Ratings. If the BV_{DSS} of the external P-channel MOSFET is momentarily exceeded, ensure the avalanche energy absorbed by the MOSFETs do not exceed the single pulse avalanche energy specification (EAS). Voltage spikes can be dampened further with a snubber.

INPUT SUPPLY AND V_{OUT} SHORTS

Input shorts can cause high current slew rates. Coupled with series parasitic inductances in the input and output paths, potentially destructive transients may appear at the input and output pins. If the short occurs on an input that is not powering V_{OUT}, the impact to the system is benign. Back-to-back P-channel MOSFETs with their common gates connected to their common sources naturally prevent any current flow regardless of the applied voltages on either side of the drain connections, as long as the BV_{DSS} is not exceeded.

If the short occurs on an input that is powering V_{OUT}, the issue is compounded by high conduction current and low impedance connection to the output via the back-to-back P-channel MOSFETs. Once the LTC4417 blocks the high input short current, V1, V2 and V3 may experience large negative voltage spikes while the output may experience large positive voltage spikes.

To prevent damage to the LTC4417 and associated devices in the event of an input or output short, it may be necessary to protect the input pins and output pins as shown in Figure 9. Protect the input pins, V1, V2 and V3, with either unidirectional or bidirectional TVS and V_{OUT} with a unidirectional TVS. An input and output capacitor between 0.1µF and 10µF with intentional or parasitic series resistance will aid in dampening voltage spikes; see Linear Technology's Application Note 88 for general consideration.

Due to the low impedance connection from V1, V2 and V3 to V_{OUT}, shorts to the output will result in an input supply UV fault. If the UV threshold is high enough and the short resistive enough, the LTC4417 will disconnect the input. The fast change in current may force the output below GND, while the input will increase in voltage.

If UV thresholds are set close to the minimum operating voltage of the LTC4417, it may not disconnect the input from the output before the output is dragged below the operating voltage of the LTC4417. The event would cause the LTC4417's internal V_{LDO} supply voltage to collapse. A 100Ω and 10nF R-C filter on V_{OUT} will allow the LTC4417 to ride through such shorts to the input and output, as shown in Figure 10. Because V_{OUT} is also a sense pin for the REV comparator, care should be taken to ensure the voltage drop across the resistor is low enough to not affect the reverse comparator's threshold. If the 1µs R-C time constant does not address the issue, increase the capacitance to lengthen the time constant.

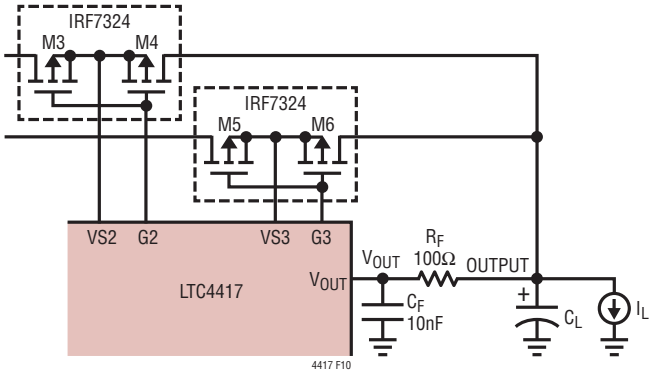


Figure 10. R-C Filter to Ride Through Input Shorts

The initial lag due to the R-C filter on the LTC4417's V_{OUT} sense and supply pin will cause additional delay in sensing when a reverse condition has cleared, resulting in additional droop when transitioning from a higher voltage to a lower voltage. If the reverse voltage duration is longer than the R-C delay, the voltage differential between the output and the filtered V_{OUT}, ΔV, can be calculated with Equation (18). I_L is the output load current during the reverse voltage condition and I_{VOUT} is current into V_{OUT}, specified in the electrical table.

$$\Delta V = \left(\frac{I_L}{C_L} \bullet C_F - I_{VOUT}\right) \bullet R_F \quad (18)$$

I_{CC} PATH SELECTION

Two separate internal power rails ensure the LTC4417 is functional when one or more input supplies are present and above 2.4V as well as limit current draw from lower

priority back up input supplies. An internal diode-OR structure selects the highest voltage input supply as the source for VB_{LDO}. If two supplies are similar in voltage and higher than the remaining input supply, the current will be equally divided between the similar voltage supplies. If all input supplies are equal in voltage, the current is divided evenly between them.

To limit current consumption from lower priority backup supplies, the LTC4417 prioritizes the internal V_{LDO}'s source supply. The highest priority source is V_{OUT}, which powers the V_{LDO} when V_{OUT} is above 2.4V. If V_{OUT} is lower than 2.4V, V_{LDO} switches to the highest valid priority input supply, V1, V2 and V3. If no input supply is valid, V_{LDO} is connected to VB_{LDO}, where the diode-OR selects highest input voltage input supply as the source. See Typical Performance Characteristics for more detail.

DUAL SUPPLY OPERATION

For instances where only two supplies are prioritized and no features of the third channel are used, ground the V3, OV3, UV3, VS3 and G3 pins of the unused channel. Alternatively, the lowest priority OV and UV comparators can be utilized for voltage monitoring when V3 and VS3 are connected to the output and G3 is left open. Figure 11 shows an example of the spare OV and UV comparators used to monitor the 5V output of the LTC3060. $\overline{VALID3}$ acts as an open drain OV/UV window comparator output.

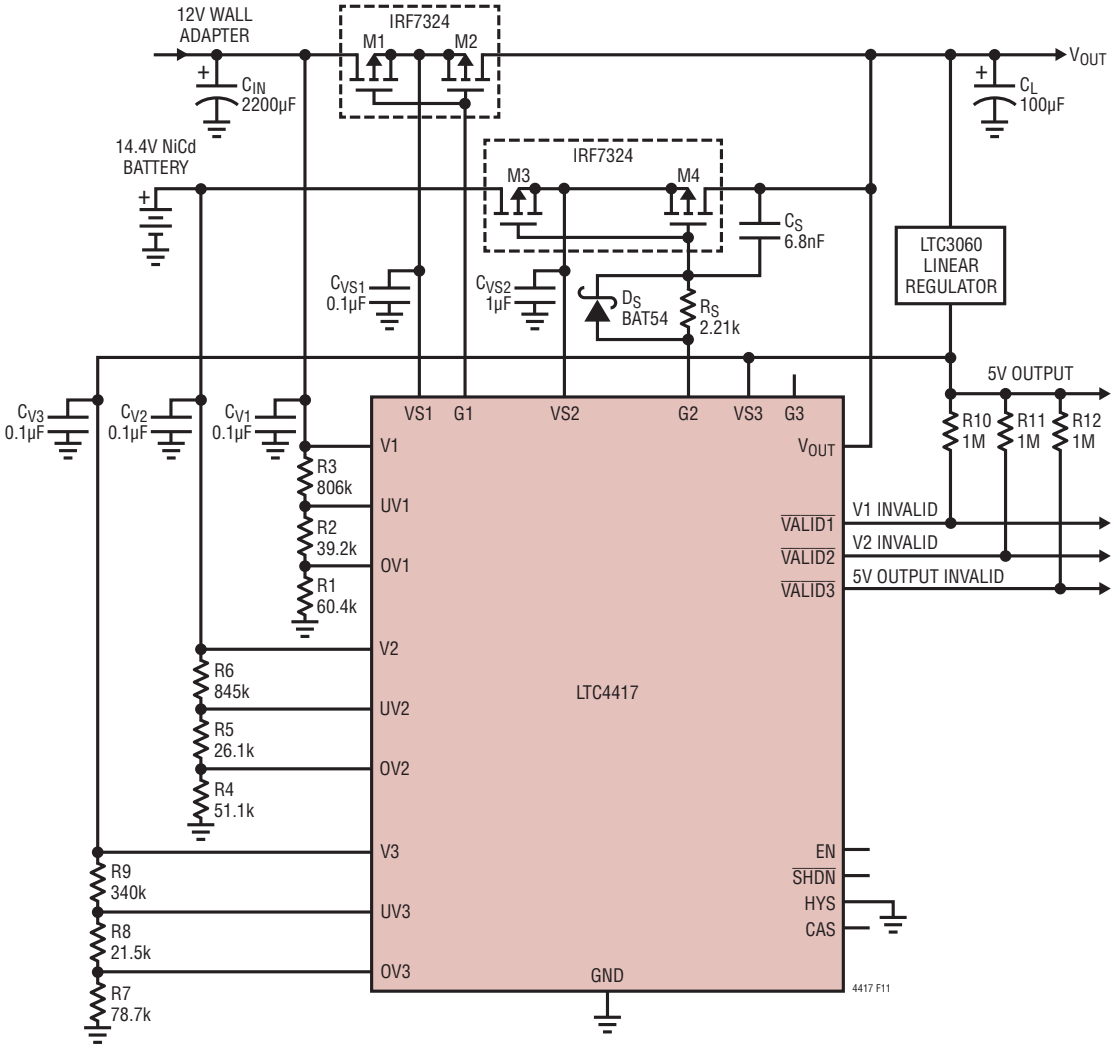


Figure 11. Dual Channel with Output Voltage Monitoring

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DISABLING ALL CHANNELS WITH EN AND $\overline{SHDN}$

Driving EN below 1V turns off all external back-to-back P-channel MOSFETs but does not interrupt input supply monitoring or reset the 256ms timers. Driving EN above 1V enables the highest valid priority channel. This feature is essential in cascading applications. For applications where EN could be driven below ground, limit the current from EN with a 10k resistor.

Forcing $\overline{SHDN}$ below 0.8V turns off all external back-to-back P-channel MOSFETs, disables all OV and UV comparators and resets all 256ms timers. $\overline{VALID1}$, $\overline{VALID2}$ and $\overline{VALID3}$ release high to indicate all inputs are invalid, regardless of the input supply condition. The LTC4417 enters into a low current state, consuming only 15µA. When $\overline{SHDN}$ is released or driven above 0.8V, the LTC4417 is required to revalidate the input supplies before connecting the inputs to V_{OUT}, as described in the Operation section. For applications where $\overline{SHDN}$ could be driven below ground, limit the current from $\overline{SHDN}$ with a 10k resistor.

CASCADING

The LTC4417 can be cascaded to prioritize four or more input supplies. To prioritize four to six supplies, use two LTC4417s with their V_{OUT} pins connected together and the master LTC4417's CAS connected to the slave LTC4417's EN as shown in Figure 12. The first LTC4417 to validate an input will soft-start the common output. Once the output is above 2.4V, power will be drawn from V_{OUT} by the other LTC4417 regardless of its input supply conditions.

When the master LTC4417 wants to connect one of its input supplies to the V_{OUT}, it simultaneously initiates a channel turn on and pulls its CAS pin low to force the slave LTC4417 to disconnect its channels. A small amount of reverse conduction may occur in this case. The amount of cross conduction will depend on the total turn-on delay of the master channel compared with the turn-off delay of the slave channel. Care should be taken to ensure the connection between CAS and EN is as short as possible, to minimize the capacitance and hence the turn-off delay of the slave channel.

When all of the inputs to the master LTC4417 are invalid, the master confirms that all its inputs are disconnected from V_{OUT} before releasing CAS. CAS is pulled to the internal V_{LDO} rail with a 20µA current source, allowing the slave LTC4417 to connect its highest valid priority channel to V_{OUT}. Confirmation that all channels are off before the slave is allowed to connect its channel to V_{OUT} prevents cross conduction from occurring.

Driving the master LTC4417's EN low forces both master and slave to disconnect all channels from the common output and continue monitoring the input supplies. Driving the master LTC4417's $\overline{SHDN}$ low places it in to a low current state. While in the low current state, all of its channels are disconnected and CAS is pulled high with a 20µA current source, allowing the slave LTC4417 to become the

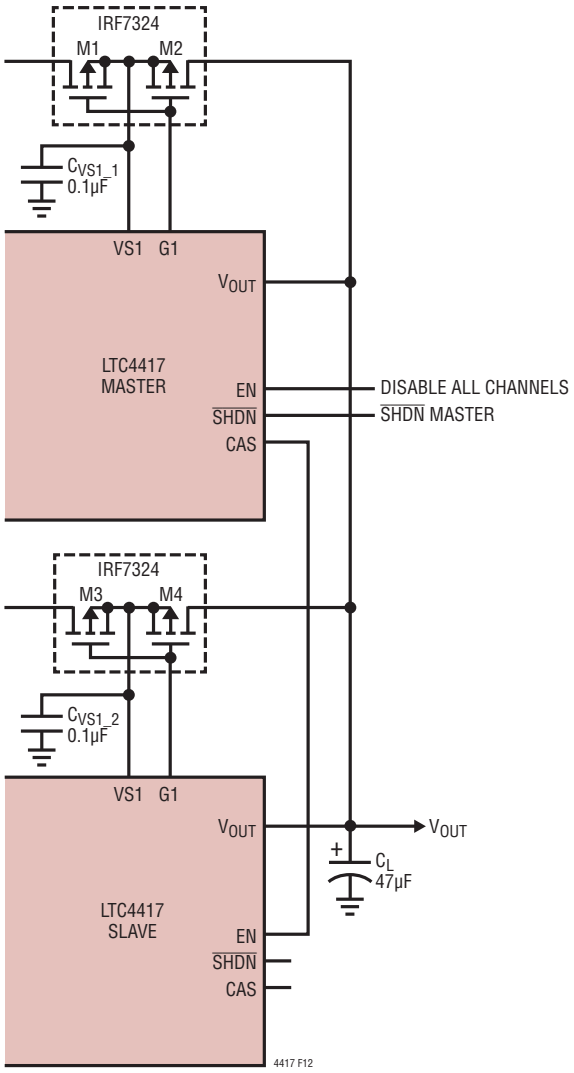


Figure 12. Cascading Application

APPLICATIONS INFORMATION

master and connect its highest valid priority channel to the common output. If seven, or more, input supplies are prioritized, additional LTC4417s can be added by connecting all individual V_{OUT} pins together and connecting each LTC4417's CAS to the next lower priority LTC4417's EN.

DESIGN EXAMPLE

A 2A multiple input supply system consisting of a 12V supply with a source resistance of 20mΩ, 7.4V main lithium-ion battery, and a backup 7.4V lithium-ion battery is designed with priority sourcing from the 12V supply, as shown in Figure 13. Power is sourced from the main battery when the 12V supply is absent and the backup battery is only used when the main battery and 12V supply are not available. The ambient conditions of the system will be between 25°C and 85°C.

The design limits the output voltage droop to 800mV during switchover. The load capacitor is assumed to have a minimum ESR of 50mΩ at 85°C and 80mΩ at 25°C through paralleling low ESR rated aluminum electrolytic capacitors. The input source is allowed to drop 1V.

Selecting External P-Channel MOSFET

The design starts with selecting a suitable 2A rated P-channel MOSFET with desired $R_{DS(ON)}$. Reviewing several MOSFET options, the low 18mΩ $R_{DS(ON)}$, dual P-channel IRF7324 with a –20V BV_{DSS}, is chosen for this application.

The low 18mΩ $R_{DS(ON)}$ results in a 72mV combined drop at 25°C and 85mV drop at 85°C. Each P-channel MOSFET dissipates 72mW at 25°C and 85mW at 85°C.

Inrush Current Limiting

When connecting a higher voltage source to a lower voltage output, significant inrush current can occur. The magnitude of the inrush current can be calculated with Equation (19).

$$I_{INRUSH} = \frac{V1 - V_{OUT(INIT)}}{R_{SRC} + ESR(C_L) + 2 \bullet R_{DS(ON)}} \quad (19)$$

where $V_{OUT(INIT)}$ is the V_{OUT} voltage when initially powered from a supply voltage less than V1, V1 is the higher voltage source, R_{SRC} is source resistance of V1, $ESR(C_L)$ is the ESR of the load capacitor, and $R_{DS(ON)}$ is the on-resistance of the external back-to-back MOSFET.

Given a total series resistance from input to output, the worst case inrush current will occur when V1 is running 20% high, at 14.4V, and V_{OUT} is at its undervoltage limit of 5.6V. During this condition, a maximum inrush current of 83A will occur, as shown in Equation (20).

$$I_{INRUSH} = \frac{14.4V - 5.6V}{20m\Omega + 50m\Omega + 36m\Omega} = 83A \quad (20)$$

Because the 83A of inrush current exceeds the 71A absolute maximum pulsed drain current rating, I_{DM}, of the IRF7324, inrush current limiting is required.

Calculating the load capacitance, C_L, and inrush current limiting circuitry component, R_S, is an iterative process. To start, use Equation (14), with $0.79 \bullet R_S \bullet C_S$ initially set to 10µs. To limit the output voltage droop to the desired 800mV, reserve 200mV for initial droop due to the load current flowing in the ESR of the output capacitor. Next, choose C_L to set the maximum V_{OUT} droop to 600mV, as shown in Equation (21).

$$C_L = \frac{2A \bullet (3\mu s + 12\mu s + 10\mu s)}{600mV} \quad (21)$$

$$C_L = 83.3\mu F$$

For margin, choose the initial C_L value equal to 100µF and use Equation (16) to determine R_S. With an allowable 1V input voltage drop and source resistance, R_{SRC}, of 20mΩ, the input voltage droop of 700mV is used to set the inrush current of 35A. The other terms in the equation come from the external P-channel MOSFET manufacturer's data sheet. The transfer characteristics curve shows the gate voltage, V_{GS}, is approximately 1.8V when driving the 35A inrush current and the capacitance verses drain-to-source voltage curve shows the maximum C_{RSS} is approximately 600pF. C_S is set to be greater than ten times C_{RSS}, or 6.8nF. To ensure the designed inrush current is lower than the absolute maximum pulse drain current rating, I_{DM}, calculate R_S using the maximum value for $\Delta V_{G(SINK)}$ and C_L, and the minimum value for C_S. For aluminum

APPLICATIONS INFORMATION

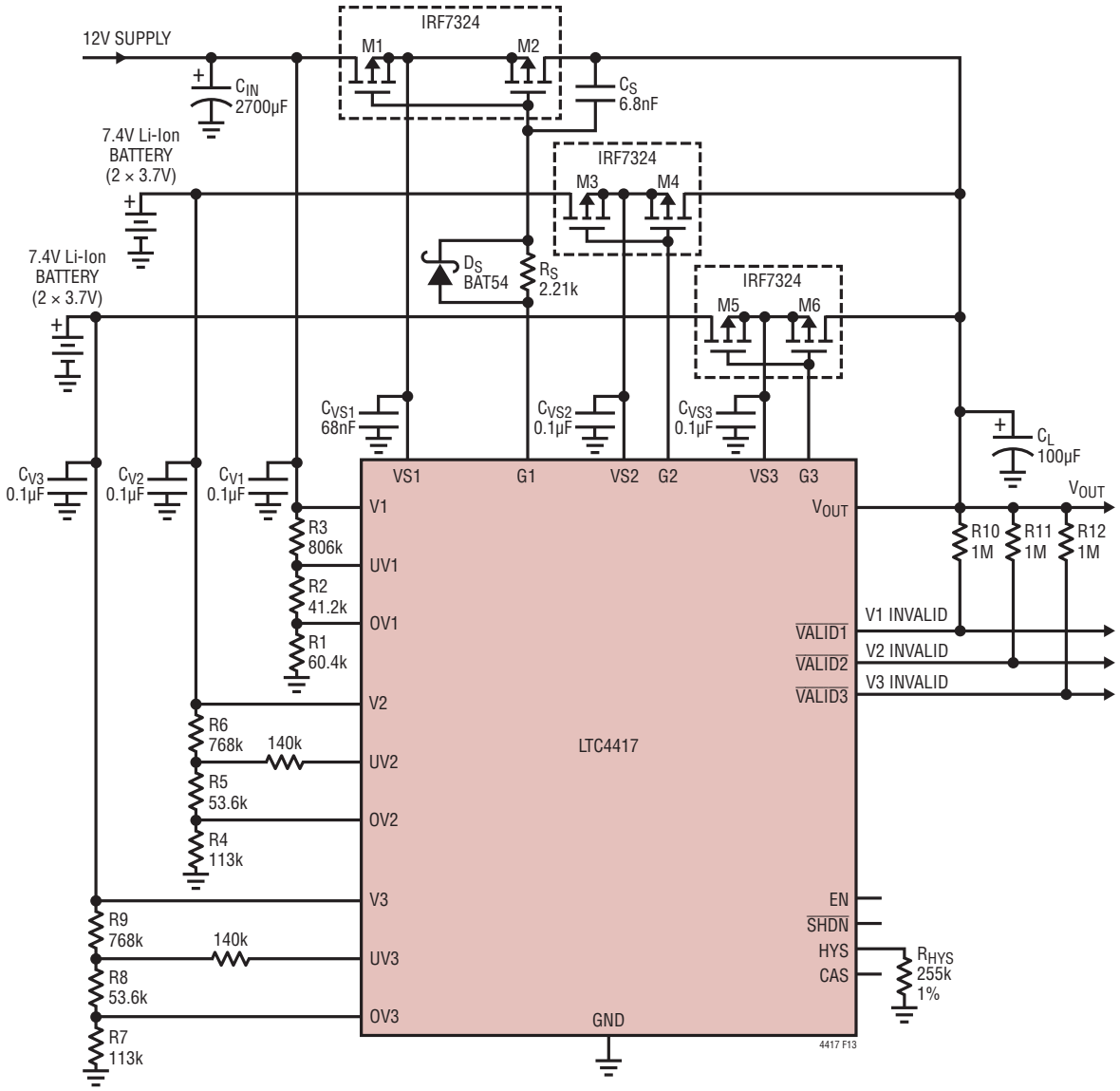


Figure 13. Industrial Hand Held Computer

electrolytic capacitors, add 20% to C_L and for ceramic NP0 C_S capacitors subtract 5%.

$$R_S = \frac{(6V - 1.8V) \bullet 120\mu F \bullet 20m\Omega}{6.5nF \bullet 700mV}$$
$$R_S = 2.22k\Omega \quad (22)$$

The standard value of 2.21kΩ is chosen for R_S and C_{VS1} is chosen to be ten times C_S or 68nF. Although 1.8V is a typical value for V_{GS}, there is sufficient margin – even if V_{GS} = 0V, the resulting I_{DM} is lower than the 71A rating.

With R_S and C_S known, the desired load capacitance with inrush current limiting is checked with Equation (14) as shown in Equation (23). Because the required load capacitance of 90µF is lower than the chosen load capacitor of 100µF, the initial choice of 100µF is suitable.

$$C_L \geq \frac{2A \bullet (3\mu s + 12\mu s + 0.79 \bullet 2.21k\Omega \bullet 6.8nF)}{600mV}$$
$$C_L \geq 90\mu F \quad (23)$$

APPLICATIONS INFORMATION

Significant power is dissipated during the channel transition time. The SOA of the P-channel MOSFET should be checked to make sure their SOA is not violated.

Worst case slew rate limited channel transition time would occur when the lithium-ion batteries are running low at 5.6V, and the supply connects while running 20% high, at 14.4V. This results in a time of 25µs, as shown in Equation (24).

$$dt = \frac{(14.4V - 5.6V) \bullet 100\mu F}{35A}$$
$$dt = 25\mu s \quad (24)$$

The IRF7324 thermal response curve at 25µs shows $Z_{\theta JA}$ to be approximately 0.18 for a single pulse. The $Z_{\theta JA}$ of 0.18 results in a maximum transient power dissipation of 694W at 25°C and 361W at 85°C. The external P-channel MOSFETs will dissipate no more than 8.8V • 37A = 325W during this period, below the available 361W at 85°C.

The initial soft-start period will also force the external back-to-back MOSFETs to dissipate significant power. To check the SOA during this period, start with Equation (9).

$$t_{STARTUP}(ms) = \frac{12V}{5[V/ms]}$$
$$t_{STARTUP}(ms) = 2.4ms \quad (25)$$

I_{MAXCAP} current of 500mA is calculated using Equation (10).

$$I_{MAXCAP} = 100\mu F \bullet 5[V/ms]$$
$$I_{MAXCAP} = 500mA \quad (26)$$

The worst case soft-start power dissipation from Equation (11) is:

$$P_{SS}(W) = 12V \bullet 500mA$$
$$P_{SS}(W) = 6W \quad (27)$$

The soft-start power dissipation of 6W is well below the calculated transient power dissipation (P_{DM}) of 79.4W at a T_C of 25°C. An ambient temperature, T_A, of 85°C results in a P_{DM} of 41.3W, indicating it is sufficient to handle the 2.4ms transient 6W power dissipation. A graphical check with the manufacturer's SOA curves confirms sufficient operating margin.

Setting Operational Range

Assuming the 12V source has a tolerance of ±20%, the input source has an operational undervoltage limit of 9.6V and an overvoltage limit of 14.4V. Ideally the UV1, UV2 and UV3 and OV1, OV2 and OV3 thresholds would be set to these limits. However, since the actual threshold varies by 1.5% and resistor tolerances are 1%, OV and UV limits must be adjusted to ±26% or 8.9V and 15.1V. Further, instead of using the internal fixed 30mV, a UV hysteresis of 200mV is set using an external hysteresis current of 250nA.

The design process starts with setting R_{HYS} using Equation (1).

$$R_{HYS} = \frac{63mV}{250nA} = 252k\Omega \quad (28)$$

The nearest standard value is 255kΩ.

Now set the UV hysteresis value using R3

$$R3 = \frac{\text{Desired Hysteresis}}{I_{OVUV(HYS)}} = \frac{200mV}{247nA} = 810k\Omega \quad (29)$$

The nearest standard value is 806kΩ.

With R3 set, the remaining resistance can be determined with

$$R1,2 = \frac{R3}{UV_{TH(FALLING)} - V_{OVUV(THR)}}$$
$$= \frac{806k\Omega}{8.9V - 1V} = 102k\Omega \quad (30)$$

R1 is

$$R1 = \frac{R1,2 + R3}{OV_{TH(RISING)}} = \frac{102k\Omega + 806k\Omega}{15.1V} = 60.1k\Omega \quad (31)$$

The nearest 1% standard value is: 60.4kΩ.

R2 is

$$R2 = R1,2 - R3 = 102k\Omega - 60.4k\Omega = 41.6k\Omega \quad (32)$$

The nearest 1% standard value is 41.2kΩ.

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Because this is a single resistive string R2, R3, and $I_{OV_UV(HYS)}$ sets the hysteresis voltage with Equation (30)

$$OV_{HYS} = (R2 + R3) \bullet I_{OVUV(HYS)} = (41.2k\Omega + 806k\Omega) \bullet 247nA = 209mV \quad (33)$$

This results in an OV threshold of 15.0V and UV threshold of 8.9V. With hysteresis, the OV_{HYS} threshold is 14.8V and the UV_{HYS} threshold is 9.1V. For the desired OV and UV 6% accuracy, 1% resistors used in this example are acceptable.

Values for R4 to R6 and R7 to R9 for V2 and V3 are similarly calculated.

Layout Considerations

Sheet resistance of 1oz copper is ~530µΩ per square. Although small, resistances add up quickly in high current applications. Keep high current traces short with minimum trace widths of 0.02" per amp to ensure traces stay at a reasonable temperatures. Using 0.03" per amp or wider is recommended. To improve noise immunity, place OV/UV resistive dividers as close to the LTC4417 as possible. Transient voltage suppressors should be located as close to the input connector as possible with short wide traces to GND. Figure 14 shows a partial layout that addresses these issues.

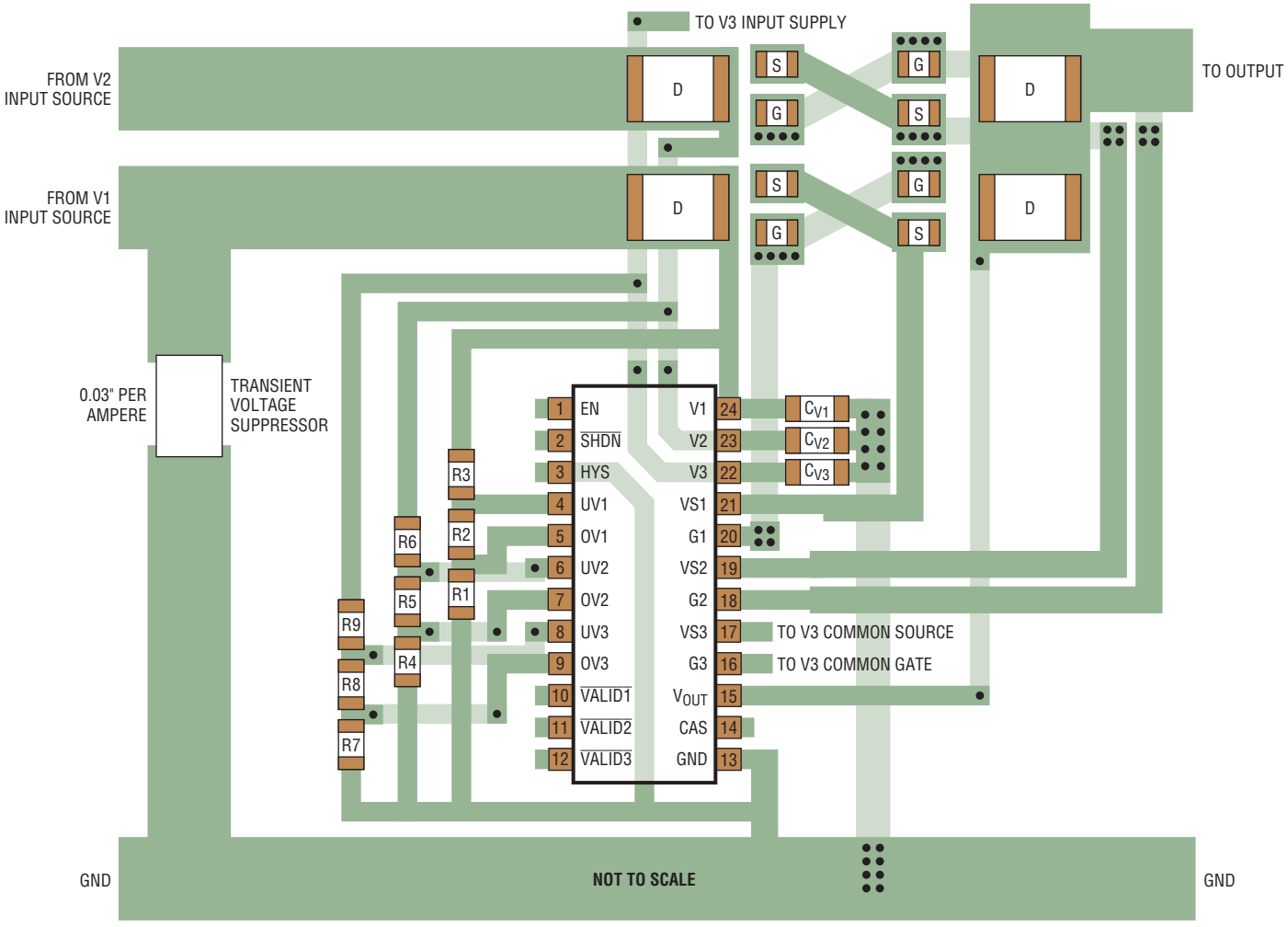
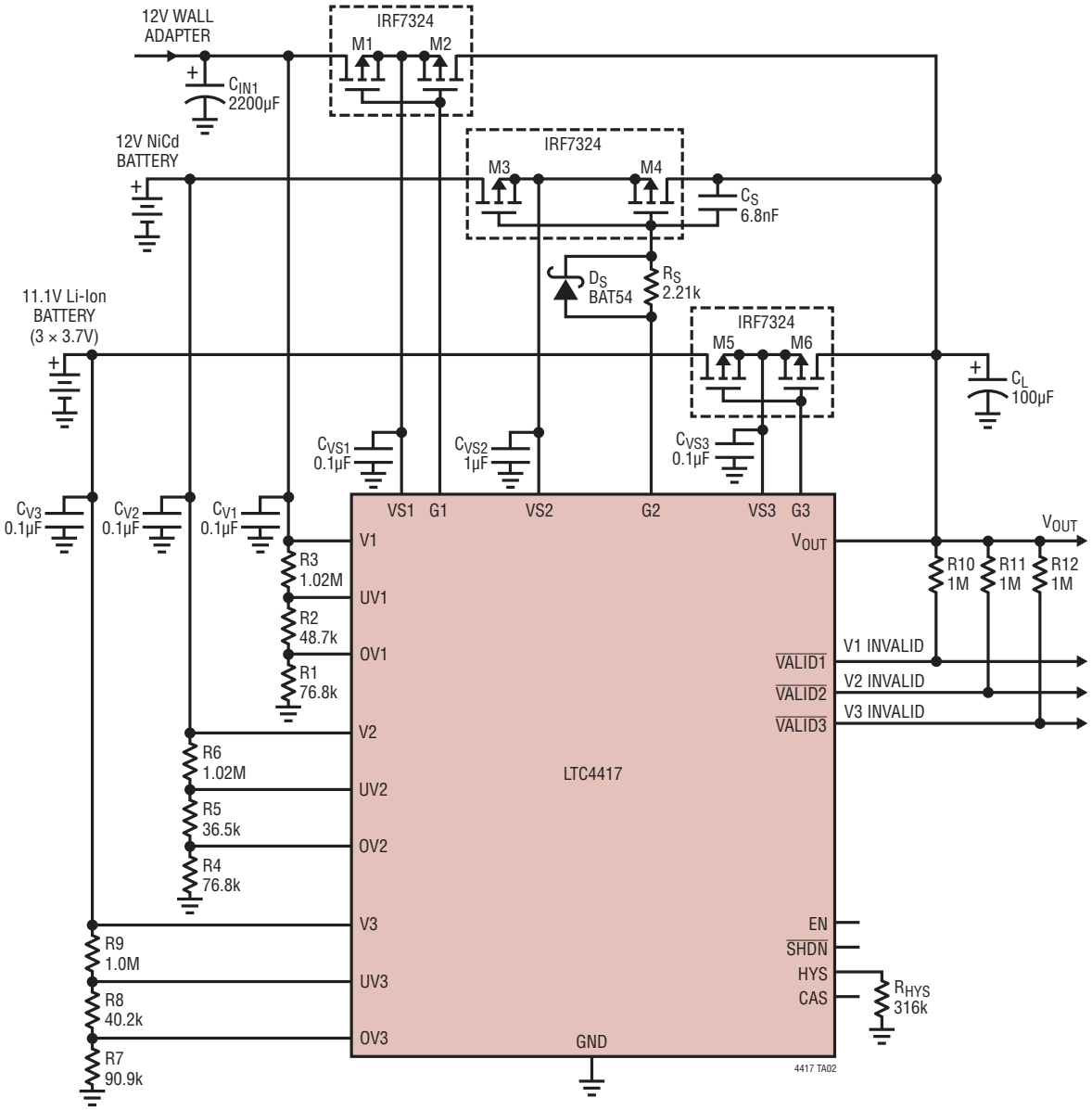


Figure 14. Recommended PCB Layout

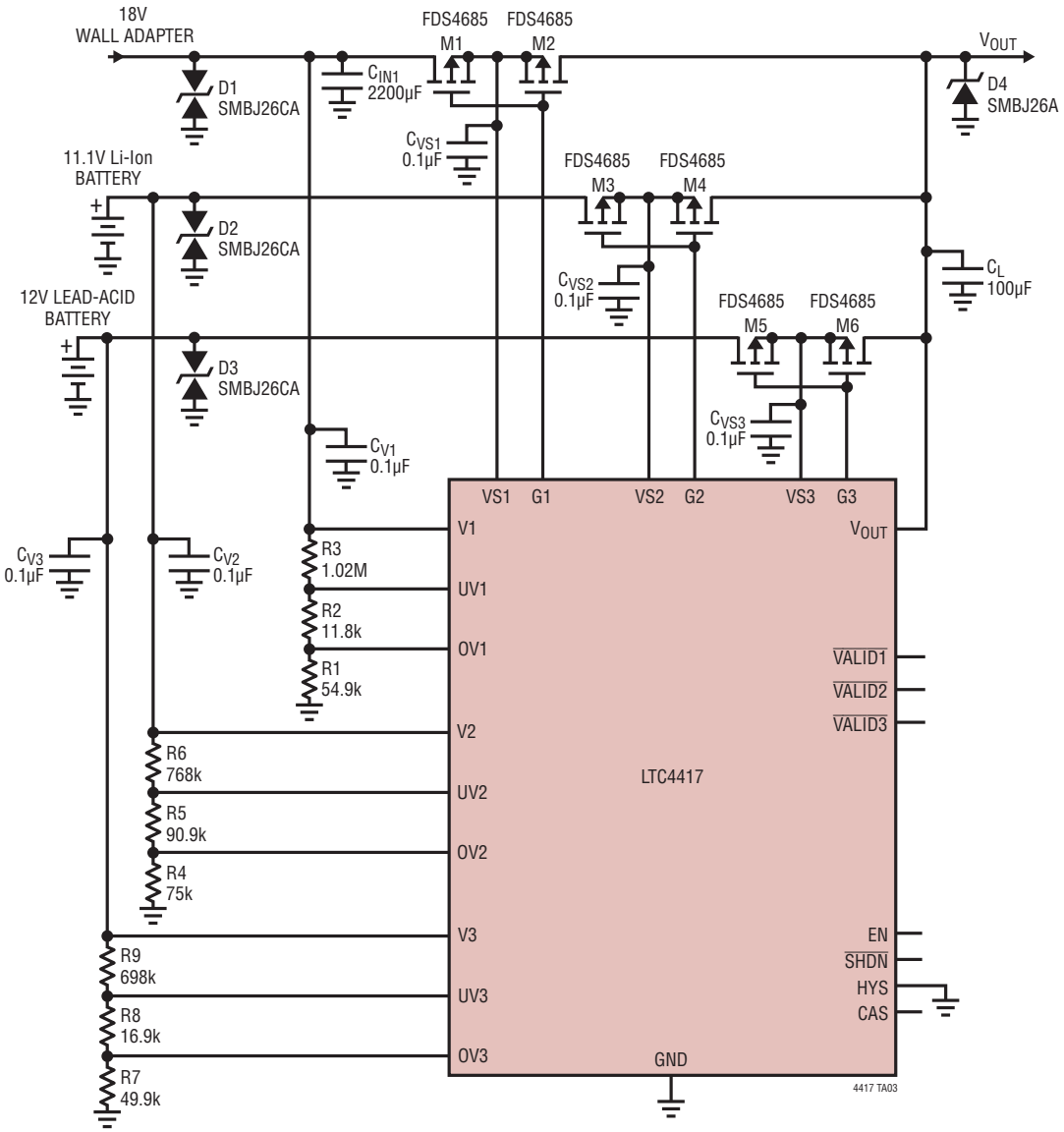
TYPICAL APPLICATIONS

12V System Using Swappable and Backup Batteries



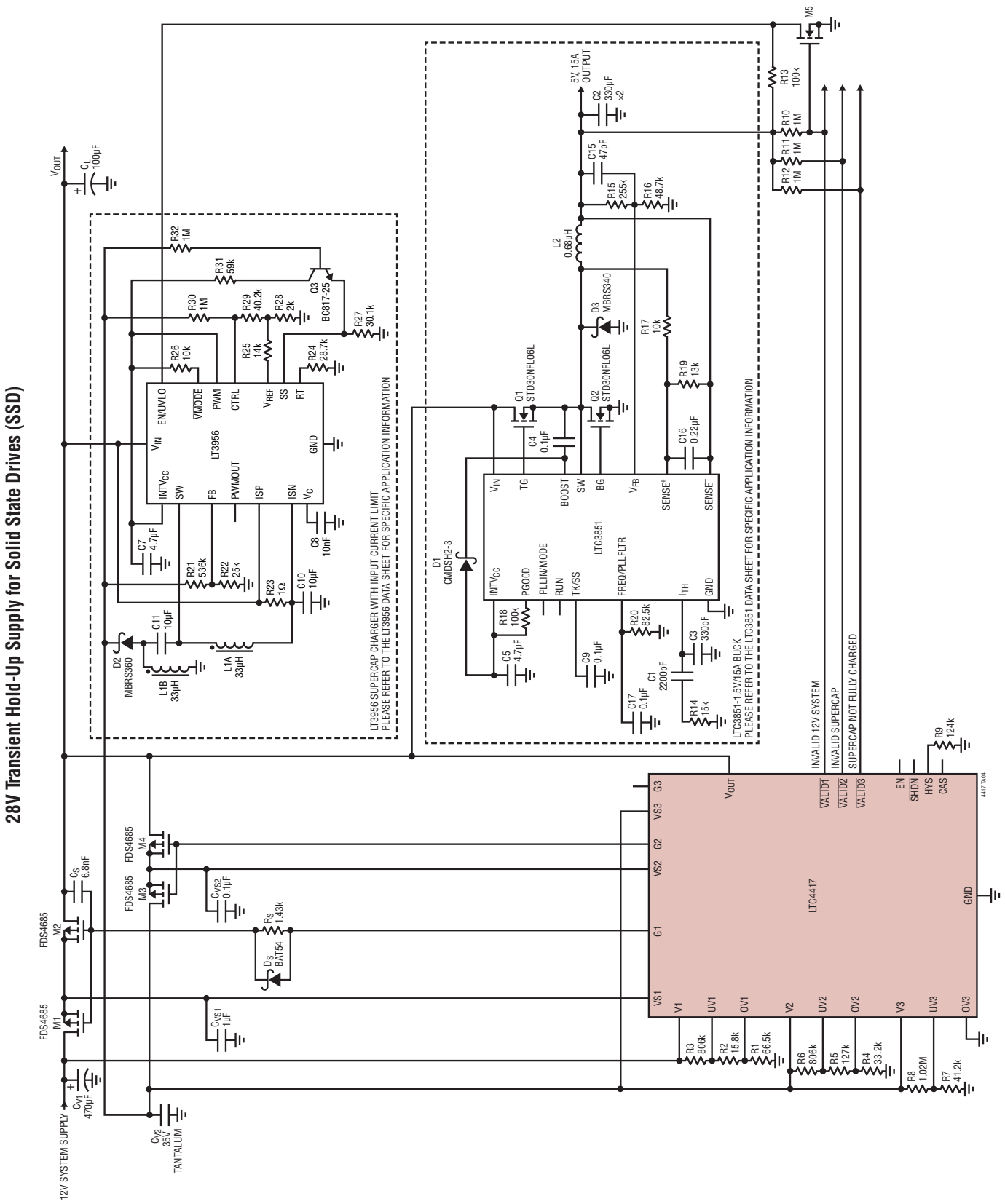
TYPICAL APPLICATIONS

18V System with Reverse Voltage Protection



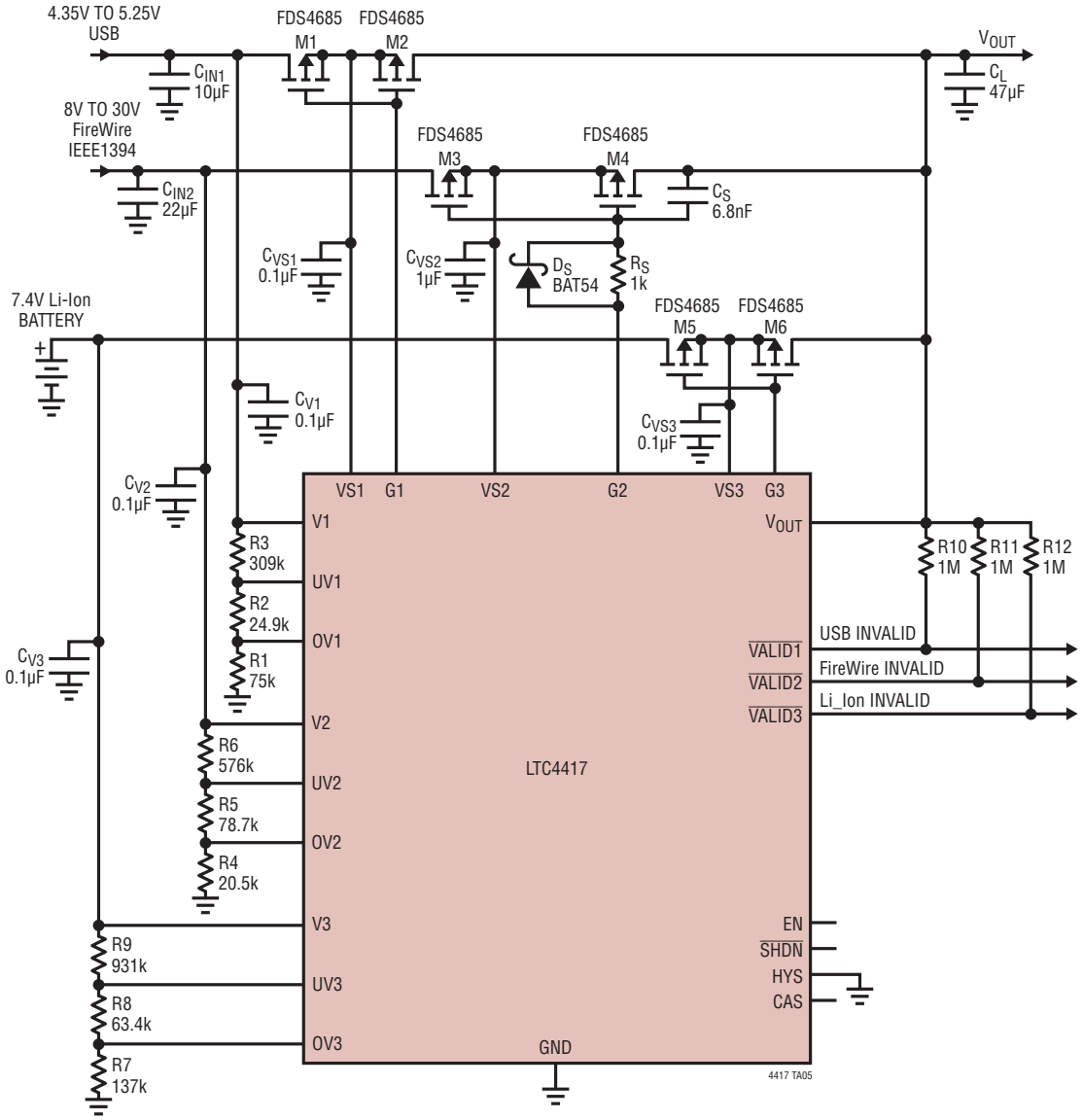
TYPICAL APPLICATIONS

28V Transient Hold-Up Supply for Solid State Drives (SSD)



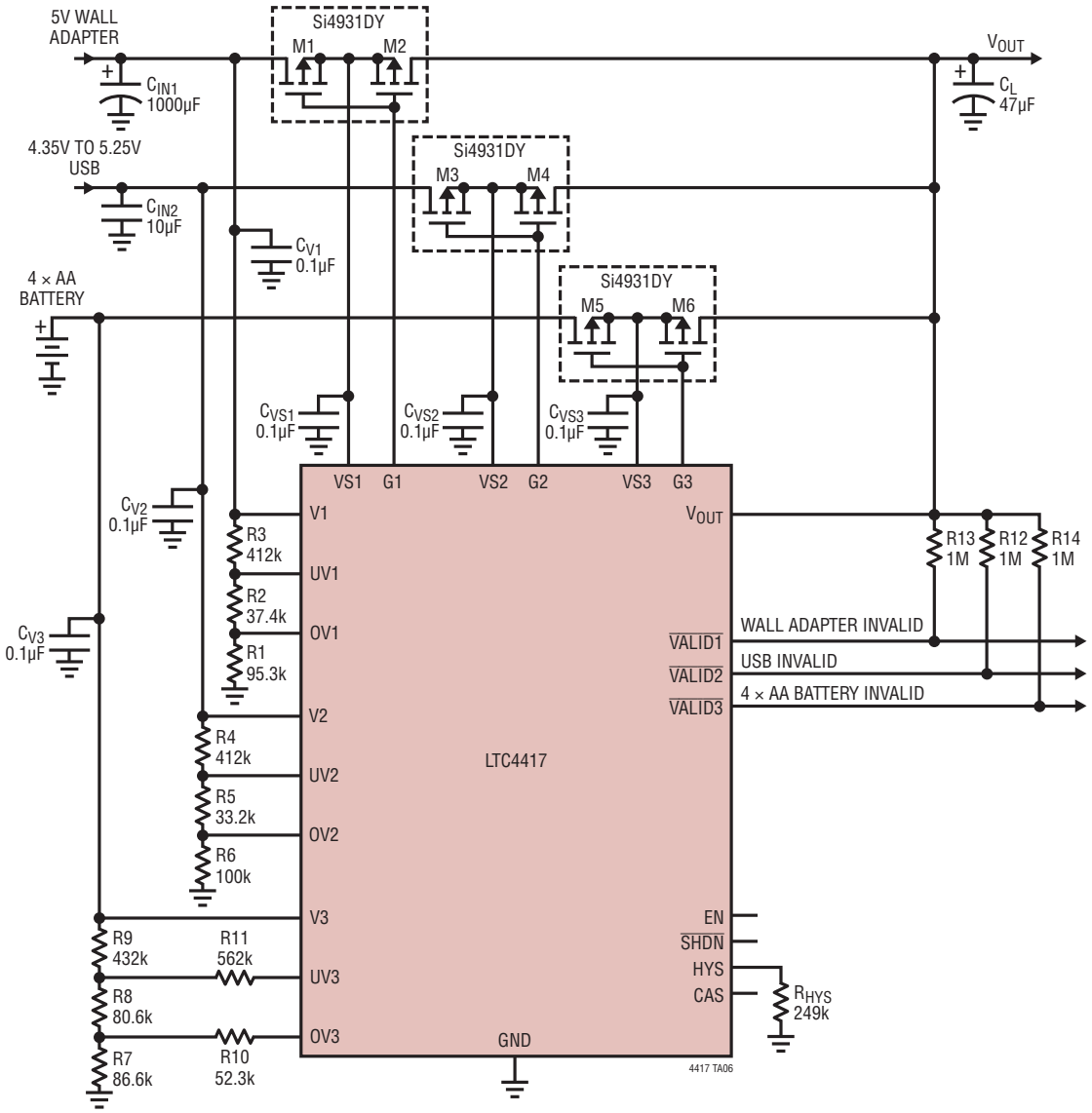
TYPICAL APPLICATIONS

Selecting from USB, FireWire, and Li-Ion Battery Power Sources



TYPICAL APPLICATIONS

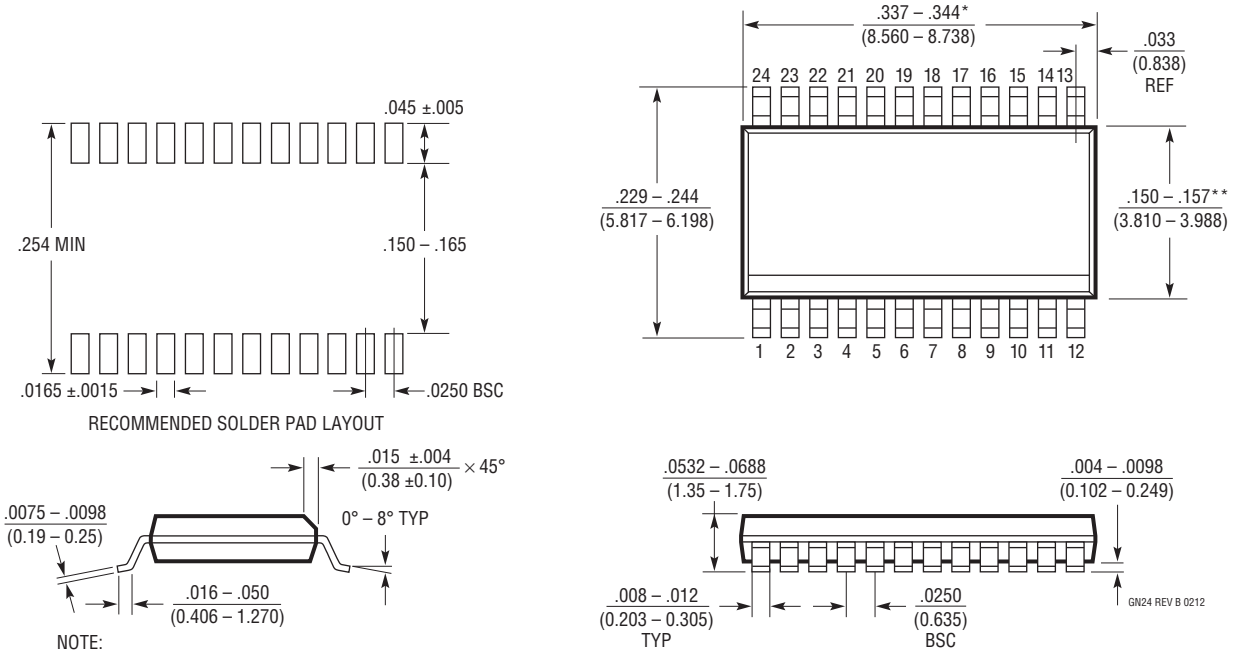
Wall Adapter and USB Input with Battery Backup



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

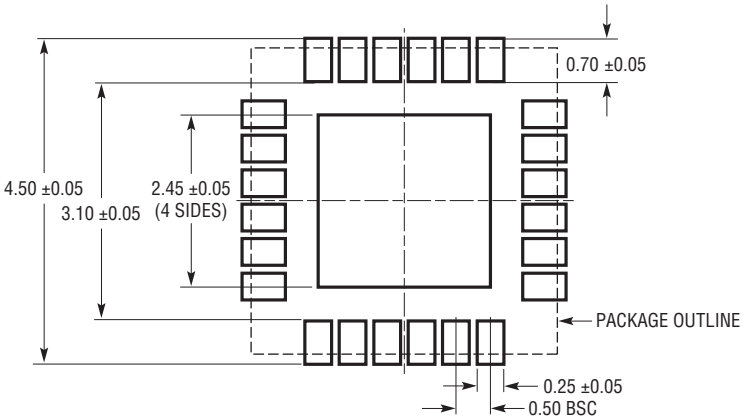
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

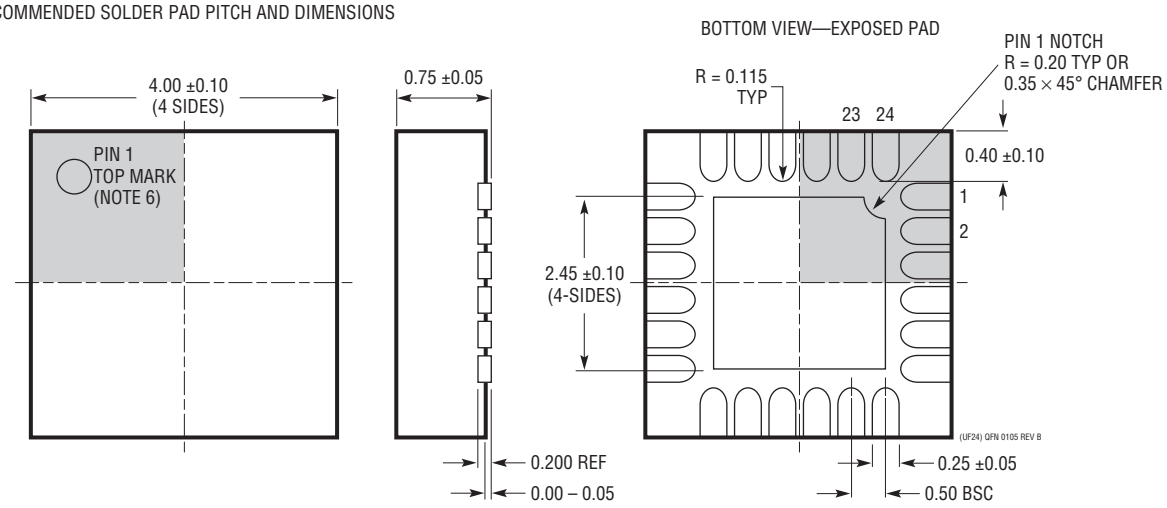
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

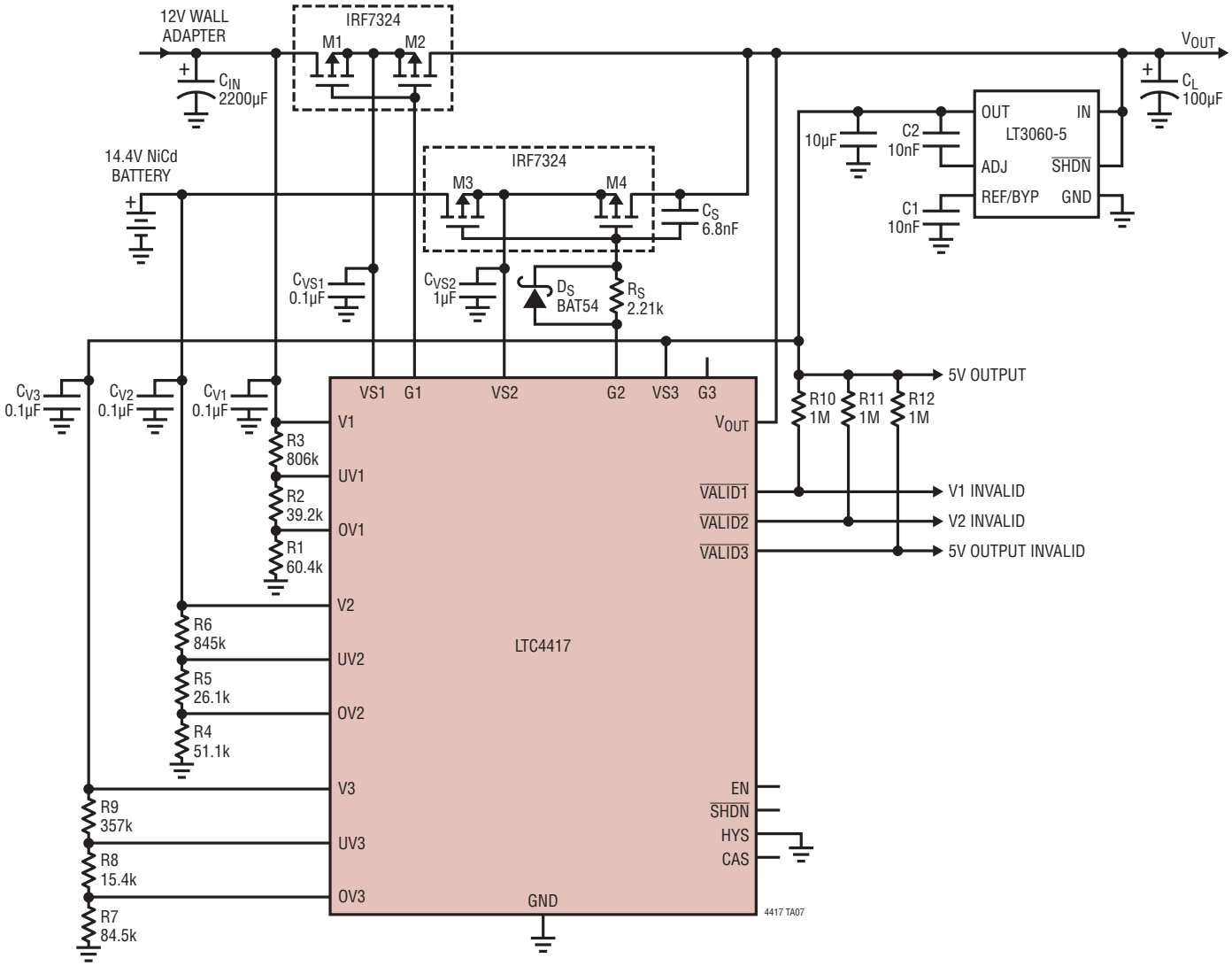


NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Dual Channel LTC4417 Application with Output Voltage Monitoring Using Third Channel



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4411	2.6A Low Loss Ideal Diode in ThinSOT™	Internal 2.6A P-channel, 2.6V to 5.5V, 40µA I_Q, SOT-23 Package
LTC4412HV	36V Low Loss PowerPath Controller in ThinSOT	2.5V to 36V, P-channel, 11µA I_Q, SOT-23 Package
LTC4415	Dual 4A Ideal Diodes with Adjustable Current Limit	Dual Internal P-channel, 1.7V to 5.5V, MSOP-16 and DFN-16 Packages
LTC4416	36V Low Loss Dual PowerPath Controller for Large PFETs	3.6V to 36V, 35µA I_Q per Supply, MSOP-10 Package
LTC4355	Positive High Voltage Ideal Diode-OR with Supply and Fuse Monitors	Dual N-channel, 9V to 80V, SO-16, MSOP-16 and DFN-14 Packages
LTC4359	Ideal Diode Controller with Reverse Input Protection	N-channel, 4V to 80V, MSOP-8 and DFN-6 Packages
LTC2952	Pushbutton PowerPath Controller with Supervisor	2.7V to 28V, On/Off Timers, ±8kV HBM ESD, TSSOP-20 and QFN-20 Packages

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LT 1112 • PRINTED IN USA
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