NuDAQ® PCI-9111DG/HR

Multifunction

Data Acquisition Card

User's Manual

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Part No: 50M-00069-1000

LEADING EDGE COMPUTING

Revision History

Revision	Release Date	Description of Change(s)
2.50	April 4, 2003	Updated release
2.6	March 16, 2022	Product update release

Preface

Disclaimer

The information in this document is subject to change without prior notice in order to improve reliability, design, and function and does not represent a commitment on the part of the manufacturer.

In no event will the manufacturer be liable for direct, indirect, special, incidental, or consequential damages arising out of the use or inability to use the product or documentation, even if advised of the possibility of such damages.

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ADLINK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental Protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

Trademarks

Product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE:	Additional information, aids, and tips that help users perform tasks.
CAUTION:	Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.
WARNING:	Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

The PCI-9111 is an advanced data acquisition card based on the 32-bit PCI bus architecture. High performance designs and state-of-the-art technology make this card ideal for data logging and signal analysis applications in areas like medicine and process control.

1.1 Features

The PCI-9111 PCI bus advanced data acquisition card provides the following advanced features:

- 32-bit PCI bus
- 12-bit analog input resolution for PCI-9111DG
  16-bit analog input resolution for PCI-9111HR
- Auto-scanning channel selection up to 256 channels
- Up to 100KHz A/D sampling rates
- 16 single-ended analog input channels
- Bipolar input signals
- Programmable gain of x1, x2, x4, x8, x16
  Input Range: ±10V, ±5V, ±2.5V, ±1.25V, ±0.625V
- On-chip sample & hold
- One 12-bit monolithic multiplying analog output channel
- 16 digital output and 16 digital input channels
- 4 extended digital input and digital output channels on the 37-pin connector
- 3 independent programmable 16-bit down counters
- Three A/D trigger modes: software trigger, programmable pacer trigger, and external pulse trigger
- Pre-trigger & Post-trigger Control
- Integral DC-to-DC converter for stable analog power source
- 37-pin D-type connector
- Compact size: half-size PCB

1.2 Applications

- Industrial and laboratory ON/OFF control
- Energy management
- Communication
- 16 TTL/DTL compatible digital input channels
- Security controller
- Product testing
- Event and frequency counting
- Waveform and pulse generation
- BCD interface driver

1.3 Specifications

<table>
<tr><th colspan="4">Analog Input (A/D)</th></tr>
<tr><td>Converter</td><td colspan="3">B.B. ADS7805 / ADS7804 or equivalent,
successive approximation type</td></tr>
<tr><td>Resolution</td><td colspan="3">12-bit/16-bit</td></tr>
<tr><td>Input Channels</td><td colspan="3">16 Single-ended</td></tr>
<tr><td>Analog Signal Input Range
(Programmable)</td><td colspan="3">Bipolar: ±10V, ± 5V, ±2.5V, ±1.25V, ±0.625V</td></tr>
<tr><td>Conversion Time</td><td colspan="3">8 μ sec</td></tr>
<tr><td>Over-voltage Protection</td><td colspan="3">Continuous ±35V max.</td></tr>
<tr><td rowspan="6">Accuracy</td><th>Gain</th><th>Range</th><th>Accuracy (mv)</th></tr>
<tr><td>1</td><td>±10v</td><td>1±0.3051</td></tr>
<tr><td>2</td><td>±5v</td><td>0.5±0.1525</td></tr>
<tr><td>4</td><td>±2.5v</td><td>0.5±0.0763</td></tr>
<tr><td>8</td><td>±1.25v</td><td>0.25±0.0381</td></tr>
<tr><td>16</td><td>±0.625v</td><td>0.25±0.019</td></tr>
<tr><td>Input Impedance</td><td colspan="3">10 MΩ</td></tr>
<tr><td>Trigger Modes</td><td colspan="3">Software, Timer Pacer, and External trigger</td></tr>
<tr><td>Data Transfer</td><td colspan="3">Pooling, FIFO half-full Interrupt</td></tr>
<tr><td>Data Throughput</td><td colspan="3">110KHz (maximum)</td></tr>
<tr><td>FIFO Depth</td><td colspan="3">1024 samples</td></tr>
<tr><th colspan="4">Analog Output (D/A)</th></tr>
<tr><td>Output Channels</td><td colspan="3">1</td></tr>
<tr><td>Resolution</td><td colspan="3">12-bit</td></tr>
<tr><td>Output Range
(jumper selectable)</td><td colspan="3">Unipolar: 0-10V
Bipolar: -10V to +10V</td></tr>
<tr><td>Converter</td><td colspan="3">DAC7541 or equivalent, monolithic multiplying</td></tr>
<tr><td>Settling Time</td><td colspan="3">30 μ sec</td></tr>
<tr><td>Linearity</td><td colspan="3">±1/2-bit LSB</td></tr>
<tr><td>Output Driving Capability</td><td colspan="3">±5mA max.</td></tr>
</table>

Digital I/O (DIO)	
Channels	16 TTL compatible inputs and outputs
Input Voltage	Low: Min. 0V, Max. 0.8V High: Min. +2.0V, Max. 5.5V
Input Load	Low: +0.8V at -0.2mA max. High: +2.7V at +20mA max.
Output Voltage	Low: Min. 0V, Max. 0.4V High: Min. +2.4V, Max. 5.5V
Driving Capacity	Low: Max. +0.5V at 8.0mA (Sink) High: Min. +2.7V at 0.4mA (Source)
Extended Digital I/O (EDIO)	
Channels	4 inputs and outputs
Input Voltage	Low: +0.8V @ -10µA max. High: +3.5V @ +10µA max.
Input Load	Low: Min: –0.5V; Max. 0.8V High: Min: +1.7V; Max. 5.75V
Output Driving Capability	Low: Max. +0.4V @ 8.0mA (Sink) High: Min. 2.4V @ 4.0mA (Source)
Programmable Counter	
A/D pacer timer	32-bit timer (two 16-bit counters cascaded together) with a 2MHz time base
Pacer Frequency Range	0.00046 Hz to 100K Hz
Pre-trigger Counter	One 16-bit counter for AD Conversion Pulse
General	
Connector	37-pin D-type connector
Operating Temperature	0°C to 60°C
Storage Temperature	-20°C to 80°C
Humidity	5% to 90% relative humidity, non-condensing
Power Requirement	+5 V @ 570 mA typical
Dimensions	105mm (H) X 175mm (L)

1.4 Software Support

ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW. All software options are included in the ADLINK All-in-One CD. Commercial software drivers are protected with licensing codes. Without the code, you may install and run the demo version for trial/demonstration purposes for only up to two hours. Contact your ADLINK dealer to purchase the software license. The ADLINK Measurement, Automation & Platform Service (MAPS) is a software service package designed for data acquisition, automation and PXI platform. By leveraging the sophisticated architecture in low-level kernel management and user friendly API, users can easily manage devices under a Windows environment and focus on developing applications.

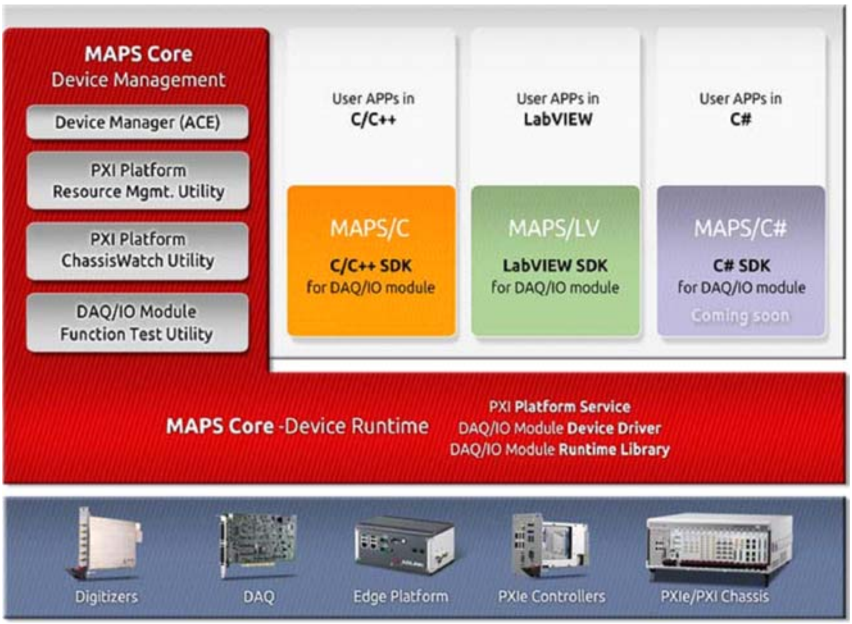

Figure 1-1: ADLINK MAPS Architecture

1.4.1 MAPS Core

ADLINK MAPS Core is a software package that includes all the device drivers for Windows and a system level management tool called ACE (ADLINK Connection Explorer). With MAPS Core installed in a user-provided PC, the operating system can identify ADLINK's devices and assign necessary resources for low-level access, such as IO read/write or direct memory access. MAPS/ Core is necessary for all ADLINK DAQ modules. To ensure the user has the latest software, go to the ADLINK product webpage or contact ADLINK technical service.

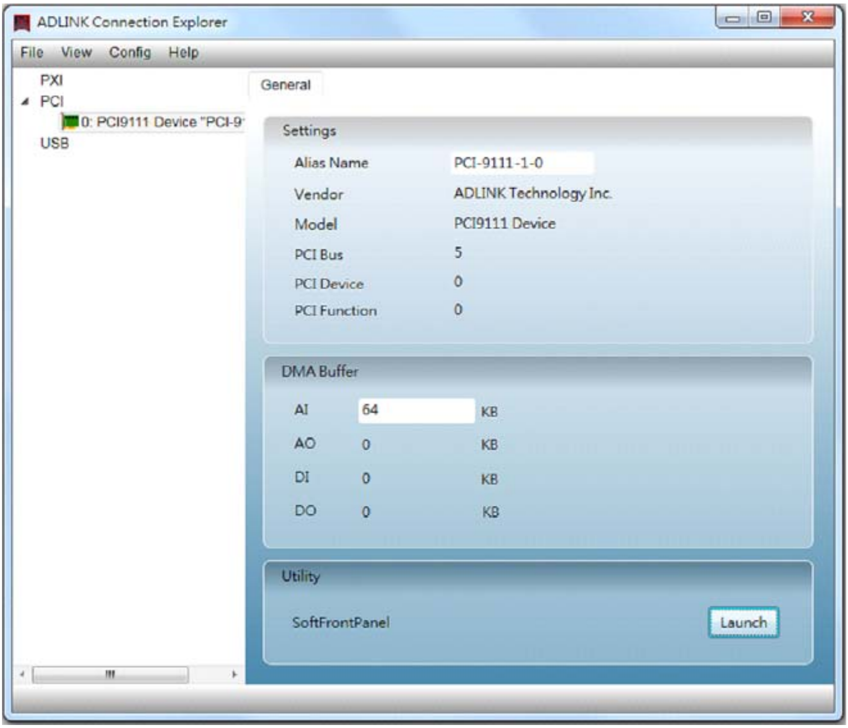

Figure 1-2: ADLINK MAPS Core

MAPS Core also comes with a system management portal called ADLINK Connection Explorer (ACE). Through ACE, users can discover and manage ADLINK DAQ modules. For example, the user can reserve a certain size of memory buffer for DMA operation or set the user alias name for operating the module in a LabVIEW environment.

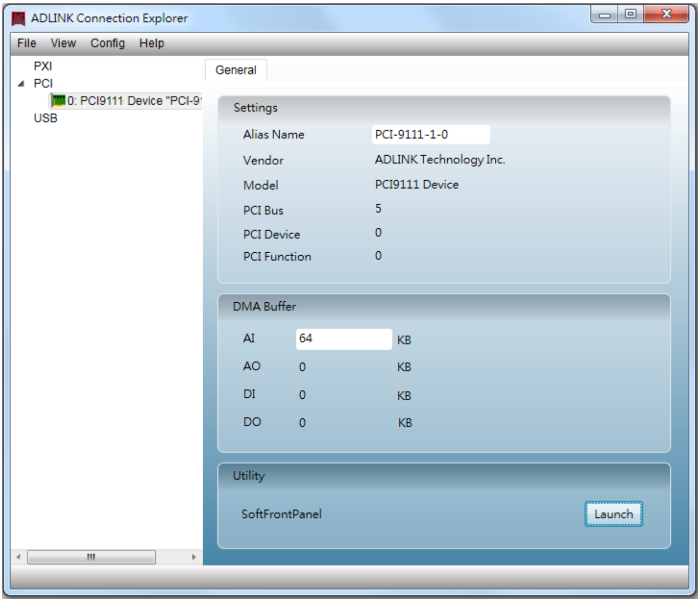

Figure 1-3: ADLINK Connection Explorer (ACE)

ADLINK Connection Explorer (ACE) also provides a ready-to-use soft-front panel for digitizer products. By clicking the Launch button in the lowest "Utility" block, this soft-front panel allows users to control digitizers through the UI and display the acquired waveform/data on the screen.

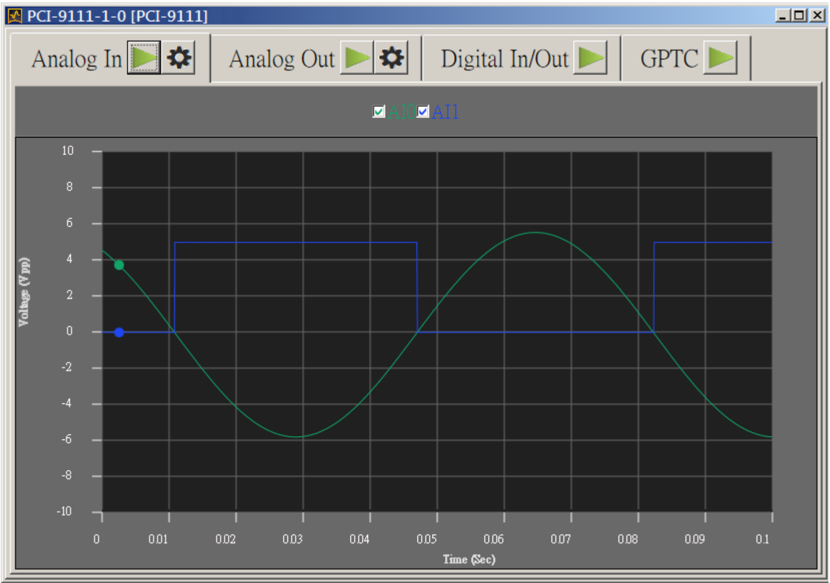

Figure 1-4: ACE Soft Front Panel

1.4.2 MAPS/LV, LabVIEW Support

Customers who develop their own programs in LabVIEW must install the MAPS/LV software package. MAPS/LV, also called DAQ-LabVIEW Plus, includes the software library and sample program for LabVIEW. For more information, download and install the latest MAPS/LV software from the following website and refer to the MAPS/LV manual:

https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_LV

1.4.3 MAPS/C, C & C++ Support

Customers who develop their own programs in C or C++ environments must install the MAPS/C software package. MAPS/C includes all the software components required for developing applications in C/C++, such as header files, a device API library and versatile sample programs for understanding how to manipulate the device correctly. Find the latest MAPS/C on the ADLINK website.

https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_C

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2 Getting Started

This chapter describes the proper installation environment, installation procedures, package contents and basic information users should be aware of.

NOTE:

Diagrams and images of equipment illustrated are for reference only. Actual system configuration and specifications may vary.

2.1 Package Contents

Before continuing, check the package contents for any damage and check if the following items are included in the packaging:

- PCI-9111 Multifunction Data Acquisition Card
- ADLINK CD
- PCI-9111 User's Manual

The card contains electro-static sensitive components that can easily be damaged by static electricity. Therefore, the card should be handled on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damage. Shipping and handling may cause damage to your module. Be sure there are no shipping and handling damages on the modules carton before continuing.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface with component side up.

Inspect the module for any damage. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

WARNING:

WARNING: DO NOT install or apply power to equipment that is damaged or if there are missing components. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/vendor immediately for assistance and obtain authorization before returning any product.

2.2 Device Layout and I/O Connectors

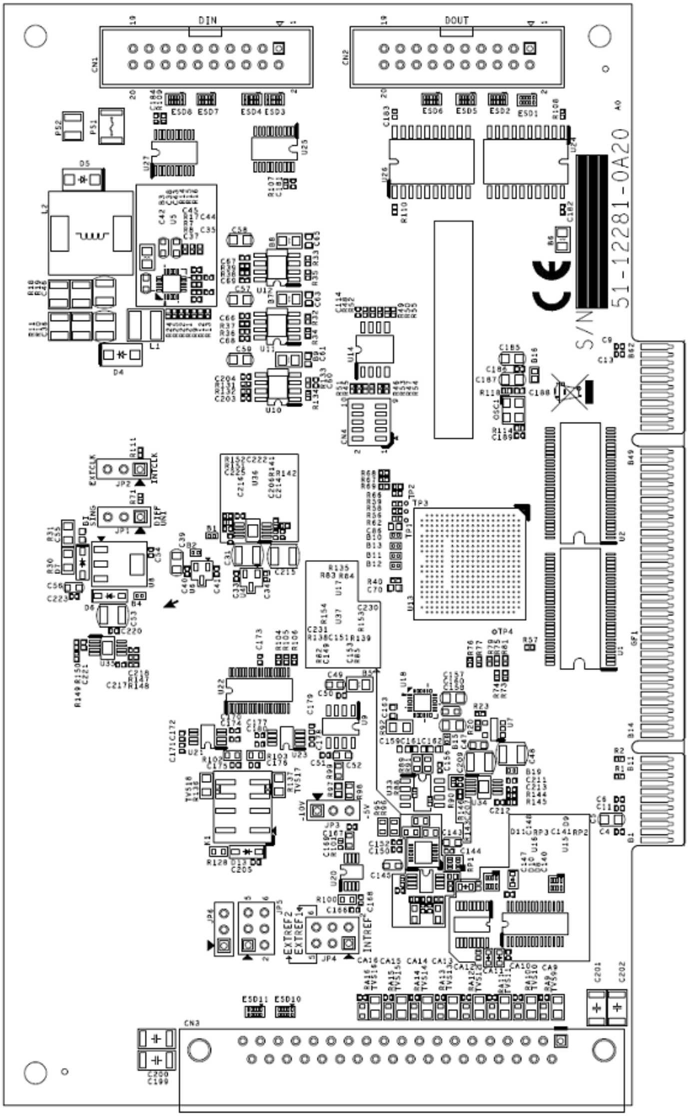


Figure 2-1: PCB Layout

2.3 Jumper Settings

There is only one configurable jumper (JP1) available on the PCI-9111 card used to set the range for the analog output channel. The analog output range can be uni-polar (0 to 10V) or bi-polar (-10V to +10V). The default setting is bi-polar. See table below for setting possibilities.

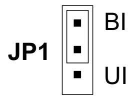
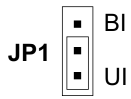
Bi-polar analog output range -10V to +10V	
Uni-polar analog output range 0V to +10V	

Table 2-1: Analog Output Range Setting

2.4 Connector Pin Assignments

The PCI-9111 comes equipped with two 20-pin insulation displacement connectors (CN1 and CN2) and one 37-pin D-type connector (CN3). CN1 and CN2 are located on the board and CN3 is located on the faceplate.

CN1 is for digital signal input, CN2 is for digital signal output, and CN3 is for analog input/output, extended digital I/O, and timer/counter signals.

2.4.1 CN1/CN2: Digital Signal Input/Output

CN1 and CN2 are 20-pin insulation displacement connectors for digital signal input/output with the following pin assignments.

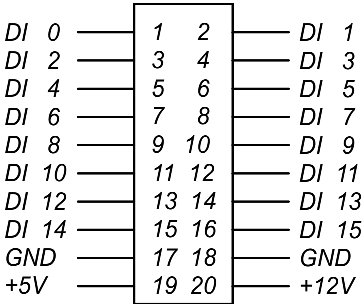


Figure 2-2: CN1 Pin Assignments

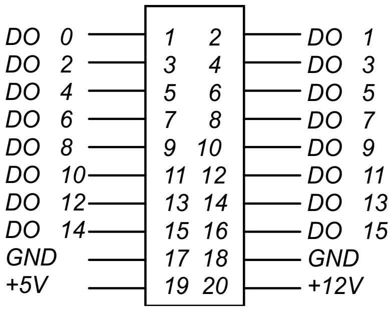


Figure 2-3: CN2 Pin Assignments

Signal Name	Description
DI n	Digital Input signal channel *n*
DO n	Digital Output signal channel *n*
GND	Digital Ground

Table 2-2: CN1/CN2 Pin Assignment Legend

2.4.2 CN3: Analog Input/Output, Extended I/O Connector

CN3 is a 37-pin D-type connector with the following pin assignments.

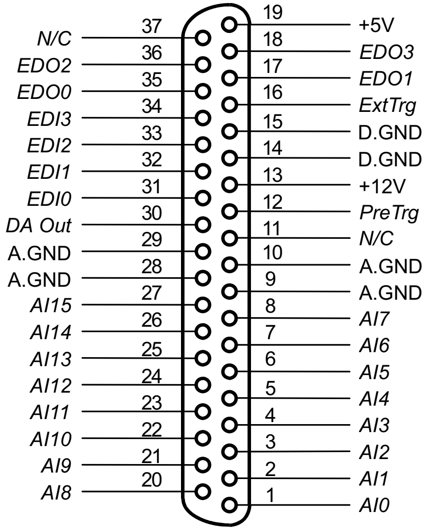


Figure 2-4: CN3 Pin Assignments

Signal Name	Description
AI n	Analog Input Channel *n* (single-ended)
DA Out	Analog Output Channel
ExtTrg	External A/D Trigger Signal
PreTrg	Pre-Trigger Stop or Post-Trigger Start Signal
EDI n	Extended Digital Input Channel n (0 to 3)
EDO n	Extended Digital Output Channel n (0 to 3)
A.GND	Analog Ground
D.GND	Digital Ground
N.C.	No connection

Table 2-3: CN3 Pin Assignment Legend

2.5 Hardware Installation Outline

2.5.1 PCI Configuration

PCI cards (or CompactPCI cards) are equipped with plug and play PCI controllers and can request base addresses and interrupts according to PCI standards. The system BIOS will install the system resources based on the PCI cards' configuration registers and system parameters (which are set by the system BIOS). Interrupt assignment and memory usage (I/O port locations) of the PCI cards can only be assigned by system BIOS. These system resource assignments are done on a board-by-board basis. It is not suggested to assign the system resource by any other methods.

2.5.2 PCI Slot Selection

A PCI card can be inserted into any PCI slot without any configuration modification to the system resources.

NOTE: The PCI system board and slot must provide bus-mastering capabilities to operate at an optimum level.

2.5.3 Installation Procedures

1. Turn off your computer.
2. Turn off all peripherals connected to your computer (printer, monitor, etc.).
3. Remove the cover from your computer.
4. Set up jumpers on the PCI or CompactPCI card.
5. Select a 32-bit PCI slot. PCI slot are shorter than ISA or EISA slots, and are usually white or ivory.
6. Before handling PCI cards, discharge any static buildup on your body by touching the metal case of the computer. Hold the edge and do not touch the components.
7. Position the board into the PCI slot you have selected.
8. Secure the card in place at the rear panel of the system.

2.6 Device Installation for Windows Systems

Once Windows 7/10 has started, the Plug and Play function of Windows system will find the new NuDAQ cards. If this is the first time the NuDAQ cards are running on your Windows system, you will be prompted to input the device information source. Please refer to the ***Software Installation Guide*** for step-by-step installation procedures.

2.7 Daughter Board Connection

The PCI-9111 can be connected with five different daughter boards. The following are compatible: ACLD-8125, 9137, 9138, 9182, 9185, and 9188. The functionality and connections are specified in the following sections.

2.7.1 Connect with ACLD-8125

The ACLD-8125 has a 37-pin D-sub connector, which can connect to the PCI-9111 through the 37-pin assemble cable. The most outstanding feature of this daughter board is the onboard CJC (cold junction compensation) circuit. You can directly connect a thermocouple to the ACL-8125 board. The CJC is only suitable for High Gain version boards.

2.7.2 Connect with ACLD-9137

The ACLD-9137 is directly connected to cards, which are equipped with 37-pin D-sub connectors. It is suitable for simple applications that do not need complex signaling conditions before an A/D conversion is performed.

2.7.3 Connect with ACLD-9182

The ACLD-9182 is a 16-channel isolated digital input board. This board is connected to CN1 of the PCI-9111 via the 20-pin flat cable. The ACLD-9182 provides 500V DC isolation voltage protection, thus protecting your PC system from damage in event that abnormal input signals occur.

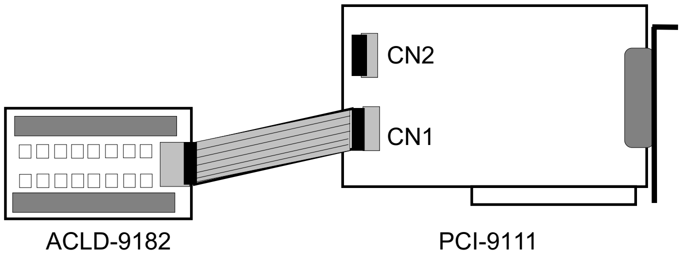
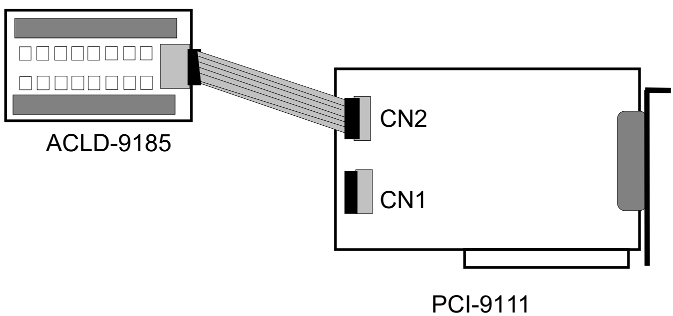


Figure 2-5: ACLD-9182 Daughter Board Connection

2.7.4 Connect with ACLD-9185

The ACLD-9185 is a 16-channel SPDT relay output board. This board is connected to CN2 of the PCI-9111 via a 20-pin flat cable. By using this board, you can control external devices through the digital output signals.



2.7.5 Connect with ACLD-9138/ACLD-9188

ACLD-9138 and ACLD-9188 are general-purpose terminal boards equipped with a 37-pin D-sub connector. The ACLD-9138 has an LED indicator to indicate the power ON/OFF status of your computer system.

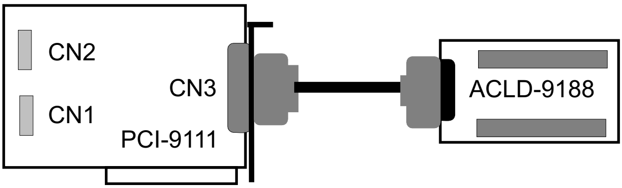


Figure 2-6: ACLD-9138/9188 Daughter Board Connection

CAUTION:

Protection on the EDI, EDO, and DA output are not provided. It is highly recommended that users implement a protection circuit of their own to avoid any possible damage to the card.

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3 Operation Theory

This chapter describes the operation theory of the PCI-9111 card functions. The functions include A/D conversion, D/A conversion, Digital I/O and counter/timer usage. The operation theory can help you to understand how to configure or to program the PCI-9111.

3.1 A/D Conversion

Before programming the PCI-9111 to perform any A/D conversions, you should have an understanding of the following:

- A/D Conversion Procedure
- A/D Trigger Source Control
- A/D Data Transfer Modes
- A/D Pre-trigger Control
- A/D Post-trigger Control
- A/D Data Format

3.1.1 A/D Conversion Procedure

To use the A/D converter, users first need to know the properties of the signal being measured. Users then can decide on which channels to use on the PCI-9111. See “Connector Pin Assignments” on page 15.

After deciding on the A/D signal source, users must decide how to trigger the A/D conversion and define/control the trigger source. The A/D converter will start to convert analog signals to a digital value when a trigger signal is on a rising edge. See “A/D Trigger Source Control” on page 29. for all possible trigger modes.

A/D data is required to be transferred to the PC's memory for further processing. The data can be read either by an I/O instruction set, which is handled directly by software, or transferred to memory via an interrupt routine. See “A/D Data Transfer Modes” on page 30. for more information regarding multi-configurations for the A/D data transfer process.

Some applications may require obtaining the data only before or after a special hardware event, in which case a Pre-Trigger is useful to stop the A/D operation. See “Pre-Trigger Control” on page 32. for configuring the PCI-9111 for Pre-Trigger Mode.

To process the A/D data, programmers should have an understanding of the A/D data format. See “Post-Trigger Control” on page 34. for details.

Analog Input Signal Connection

The PCI-9111 provides 16 single-ended analog input channels. The analog signal can be converted to digital value by the A/D converter. To avoid ground loops and to obtain accurate measurements of A/D values, it is important to understand the signal source type. The single-ended mode has only one input relative to ground and is suitable for connecting with a *floating signal source*. A floating source is one that does not have any connection to ground. Figure 3-1 shows a single-ended connection. Note that when more than two floating sources are connected, the sources must have a common ground.

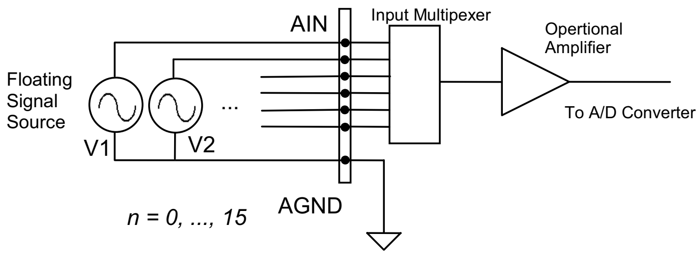

Figure 3-1: Analog Input Signal Connection

Signal Channel Control

There are two ways to control the channel number, either by a software program or by auto channel scanning which is controlled by the ASCAN bit in the AD mode control register. As ASCAN is cleared (0), the value of the AD channel MUX register defines the channel to be selected. Only one channel can be selected in this situation.

When ASCAN is set (1), the value in the AD channel MUX register defines the ending channel number of the auto-scanning operation. Under auto scan mode, the channels are scanned from channel 0 to the ending channel. Whenever a trigger signal is on the rising edge, the channel number to be selected will increase automatically. For example, if the ending channel number is 3, the auto channel scanning sequence is 0, 1, 2, 3, 0, 1, 2..., until the ASCAN bit is cleared.

NOTE:

- The current A/D channel number can be read back from the A/D data register on the 12-bit PCI-9111DG but it is not possible with the 16-bit PCI-9111HR.
- The MUX register is 8 bits long. The 4 LSB is used to select the multiplexer onboard. The 4 MSB can be sent out via the EDO pins of the CN3 connector to select an external daughter board. At most 16-daughter boards can be selected and a total of 256 channels can be selected without extra circuits.

Signal Range

A properly define signal range is important in any data acquisition process. The input signal may be saturated if the A/D gain is too large or the resolution may be not enough if the signal is small. The maximum A/D signal range of the PCI-9111 is +/- 10 volts when the A/D gain value is 1. The A/D gain control register controls the maximum signal input range. The signal gain is programmable with 5 levels (1, 2, 4, 8, 16). The signal ranges of the 16 channels are identical at all times.

The available signal polarity on PCI-9111 is bi-polar. However, the bi-polar input range can still cover a uni-polar application. In addition, the high resolution of the PCI-9111HR can cover most applications.

3.1.2 A/D Trigger Source Control

There are 3 different trigger conditions available to the PCI-9111. The different trigger conditions are specified below.

Software Trigger

The trigger source is software controllable in this mode. That is, the A/D conversion is started when any value is written into the software trigger register. This trigger mode is suitable for low speed A/D conversions. Under this mode, the timing of the A/D conversion is fully controlled by the software. However, it is difficult to control a fixed A/D conversion rate unless another timer interrupt service routine is used to generate a fixed rate trigger.

Timer Pacer Trigger

The onboard timer/counter chip is used to provide a trigger source for an A/D conversion at a fixed rate. Two counters are cascaded together to generate a trigger pulse at precise periods. See “Timer/Counter Operation” on page 42. for timer/counter operations. This mode is ideal for high speed A/D conversion. It can be combined with the FIFO half full interrupt or EOC interrupt to transfer data. The A/D trigger, A/D data transfer and Interrupt can be set independently, thus most complex applications can be covered. It's recommended that this mode be used if the application requires a fixed and precise A/D sampling rate.

External Trigger

Through Pin 16 of CN3 (ExtTrig), an A/D conversion can also be triggered by an external signal. The A/D conversion starts when ExtTrig changes from a high to a low level. The conversion rate in this mode is more flexible depending on the available trigger options of the external device. The external trigger can be also combined with the FIFO half interrupt, EOC interrupt or program FIFO polling for transferring data.

3.1.3 A/D Data Transfer Modes

The A/D data are buffered in the FIFO memory. The FIFO size of the PCI-9111 is 1024 (1K) words. If the sampling rate is 100 KHz, the FIFO can buffer 10.24 ms of analog signal. Data transferred to the FIFO after the FIFO is full will be lost. The software must read out the FIFO data before it becomes full.

The data must be transferred to the host memory after the data is ready and before the FIFO is full. With the PCI-9111, different transfer modes can be used. The different transfer modes are described below.

Software Data Polling

Software data polling is the easiest way to transfer A/D data. This mode can be used with software A/D trigger mode. After the A/D conversion is triggered by software, the software should poll the FF_EF bit of the A/D status register until it becomes low level.

If the FIFO is empty before the A/D start, the FF_EF bit will be low. After the A/D is completed, the A/D data is written to FIFO immediately, therefore the FF_EF becomes high. You can consider the FF_EF bit as converted data ready status. That is, when FF_EF is high, the data is ready. Note that, while A/D is being converted, the ADBUSY bit is low. After A/D conversion, ADBUSY becomes high to indicate it is not busy. **DO NOT** use this bit to poll the AD data.

It is possible to read A/D converted data without polling. The A/D conversion time will not exceed 8.5μs on the PCI-9111 card. Hence, after a software trigger, the software can wait for at least 8.5μs then read the A/D register without polling.

Data polling transferring is suitable for applications that need to process AD data in real time. Especially when combining with the timer interrupt generation, the timer interrupt service routine can use the data polling method to get multi-channel A/D data in real time under fixed data sampling rates.

FIFO Half-Full Interrupt Transfer

Sometimes, applications do not need real-time processing, but the foreground program is too busy to poll the FIFO data. This is when the FIFO half-full interrupt transfer mode is useful. In addition, as the external A/D trigger source is used, the sampling rate may not be easy to predict, then the method can be applied because the CPU is only interrupted when the FIFO is half-full, thus reserving CPU load.

Under this mode, an interrupt signal is generated when FIFO becomes half-full, meaning there is 512 word data in the FIFO already. The ISR can read a block of data at every time an interrupt occurs. This method is convenient for reading the A/D In size of a “block” (512 words) and is beneficial for software programming.

3.1.4 Pre-Trigger Control

In certain applications, data acquisition is applied and stops under a special hardware signal. Without the Pre-Trigger function, the software can start the A/D at any time, but it is very difficult to stop the A/D in real-time with software. Under “Pre-Trigger” mode, the pre-trigger (PTRG) signal (from Pin 12 of CN3) and the 0 counter are used to “STOP” the A/D sampling.

After setting up the Pre-Trigger mode, the hardware is continuously acquiring A/D data and waiting for the pre-trigger signal. Before the pre-trigger signal is inserted, the software must read the FIFO data to prevent FIFO becoming full. Additionally, software should store usable data as much as possible to the host PC‘s memory.

When the pre-trigger signal is inserted, the counter starts to count down from the initial counter value N to count the number of the A/D conversion trigger signal. The A/D trigger will be disabled automatically when the counter value reaches zero. The value of N can be 1 to 65535 and the last N A/D data is sampled after the pre-trigger signal. The software must continuously read data out from the FIFO to prevent the FIFO becoming full. The software also should poll the counter value to check if the A/D sampling has stopped.

To set up Pre-Trigger mode, the following steps should be followed.

1. Set Pre-Trigger Mode Off: PTRG = OFF.
2. Set Counter #0 value N (N=1-65535). Note that the larger the counter value, the more host memory buffer is needed.
3. Set up A/D data acquisition, including, A/D range, channel scan, data transfer mode and so on.
4. Set Pre-Trigger Mode On: PTRG = ON.
5. Read A/D data into host PC memory buffer with a data transfer method, otherwise the FIFO will become full. At the same time, wait for the pre-trigger signal and check if the Counter # 0 value is down to zero.
6. If A/D has stopped, set the Pre-Trigger Mode off and process the data stored in the host memory.
7. Go to Step 1 to set the Pre-Trigger mode and wait for the next pre-trigger event.

The Pre-Trigger timing is shown as follows.

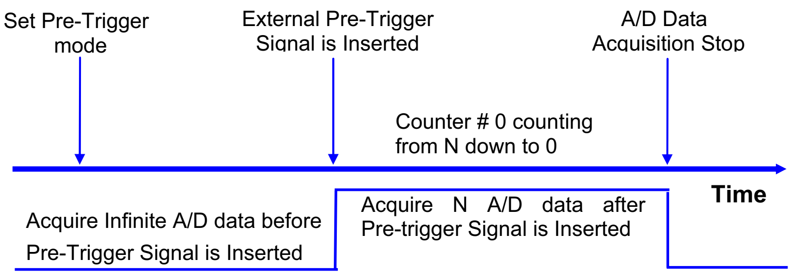

Figure 3-2: Pre-Trigger Timing

If the application acquires data after the pre-trigger signal, only the last N data needs to be stored. The maximum value of N is 65535. If the application only needs to acquire data before the pre-trigger signal, set N=1, then just one more data will be sampled after pre-trigger signal and infinite data before pre-trigger signal can be stored.

3.1.5 Post-Trigger Control

Another useful trigger mode is Post-Trigger. Under “Post-Trigger” mode, the post-trigger (POTRG) signal (from Pin 12 of CN3) is used to “START” the A/D sampling.

After setting up Post-Trigger mode, the A/D converter will not acquire data until the post-trigger signal is asserted. Users can poll the FIFO empty bit (FF_EF) to detect whether the Post-Trigger signal is asserted or not. Once the post-trigger is asserted, the hardware will begin to acquire data. Different from Pre-Trigger control mode, users can acquire data continuously until the Post-Trigger mode is disabled.

The following steps can be referenced for Post-Trigger control

1. Disable all A/D trigger sources, e.g.: Timer-Pacer / Software trigger (TPST = 0) and External / Internal trigger (EITS = 0). Set Post-Trigger mode ON: POTRG = ON.
2. Set up A/D data acquisition, including, A/D range, channel scan, data transfer mode and so on.
3. Reset FIFO.
4. Enable the selected A/D trigger source (Timer-Pacer, Software or external trigger).
5. Waiting for Post-Trigger signal to be asserted. Users can poll the FIFO empty bit to see if the post-trigger signal has started.
6. Once the post-trigger signal is asserted, data processing begins. To stop data acquisition, disable the A/D trigger source.
7. Go to step 1 to start the next Post-Trigger acquisition.

The Post Trigger timing is shown as follows.

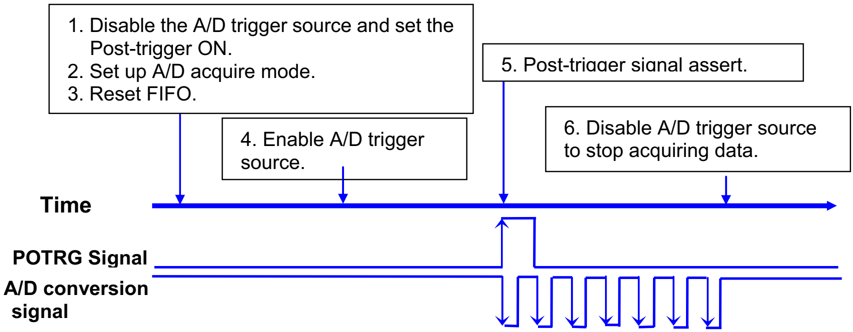

Figure 3-3: Post Trigger Timing

Under pre-trigger or post-trigger control schemes, the TRGEVENT flag signal can come in handy. When the pre-trigger or post-trigger signal is inserted, the TRGEVENT will be set to 1. After an acquisition or before the next trigger signal is inserted, the trigger event flag must be cleared by the user in order to set the correct flag status for the next incoming trigger event.

NOTE: Either the pre-trigger mode or post-trigger mode can be enabled at any one time, but not both. The post-trigger mode is only available with hardware revision B2.

3.1.6 A/D Data Format

The A/D data read from the FIFO is in two formats. As the A/D gain is 1, the A/D signal range is roughly +10V to -10V bi-polar. In the PCI-9111HR, the whole 16-bit A/D data are available. The relationship between voltage and the A/D data value is shown in the following table.

A/D Data (Hex)	Decimal Value	Voltage (Volts)
7FFF	+32767	+9.99969
4000	+16384	+5.00000
0001	1	+0.00031
0000	0	0.00000
FFFF	-1	-0.00031
C000	-16384	-5.00000
8001	-32767	-9.99969
8000	-32768	-10.00031

Figure 3-4: Relationship between voltage and A/D data value

NOTE:

The decimal value of the A/D data is in the same sign with the bi-polar voltage. Therefore, the sign extension conversion is not necessary.

The A/D converted data of the 12-bit PCI-9111DG is on the 12 MSB of the A/D data. The 4 LSB of the 16 bits A/D data are the channel number and must be truncated by the software. The relationship between voltage and the A/D converted data value is shown in the following table.

A/D Data (Hex)	Decimal Value	Voltage (Volts)
7FF	+2047	+9.9951
400	+1024	+5.0000
001	1	+0.0049
000	0	0.0000
FFF	-1	-0.0049
C00	-1024	-5.0000
801	-2047	-9.9951
800	-2048	-10.0000

Figure 3-5: Relationship between voltage and A/D converted data

The formula between the A/D converted data and the voltage value is:

$$Voltage = AD\_data \times \frac{1}{K} \times \frac{10}{gain}$$

Where *gain* is the value of the A/D gain control register, *K=32768* for PCI-9111HR, and *K=2048* for PCI-9111DG.

3.2 Extended Digital I/O Port

There are 4 extended digital input (EDI) signals and 4 extended digital output (EDO) signals on theCN3 connector. The 4 EDI signals are dedicated as input signals, however the 4 EDO signals can be used as digital input (Mode 1), digital output (Mode 2) or channel number output (Mode 3).

Note that when setting the EDO function as channel number output (Mode 3), it presents the high nibble (4 MSBs) of the channel number whether using manual scan, or auto scan mode.

3.3 D/A Conversion

The PCI-9111 has one analog output channel. The signal range can be uni-polar or bi-polar, set by JP1.

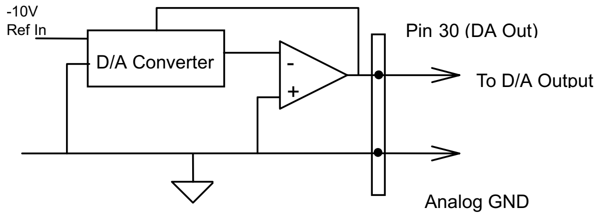

Figure 3-6: D/A Conversion Circuit

The operation of the D/A conversion is much simpler than the A/D operation. You only need to write a digital value into the D/A data registers and the corresponding voltage will be outputted on DAOut (Pin 30 of CN3). The mathematical relationship between the digital data *DAn* and the output voltage is formulated as follows.

$$V_{out}=\text{span x DAn / 4096– Unipolar}$$

$$V_{out}=\text{span x DAn / 4096 + (-10)– Bipolar}$$

Where *span* is the span in volts. If your output range is -10V to 10V (Bipolar), then span is 20; if your output range is 0 to 10V (Unipolar), then span is 10. *Vout* is the output voltage, and *DAn* is the digital data value in the D/A data registers.

Before performing the D/A conversion, users should take note of the D/A output range, which is set by JP1. See “Jumper Settings” on page 14.

Digital Data Input	**Analog Output**	
	Unipolar 0V to 10V	**Bipolar -10V to 10V**
FFF hex	+9.9976V	+9.9951V
800 hex	+5.0000V	0.0000V
7FF hex	+4.9976V	-0.0049V
000 hex	0.0000V	-10.0000V
1 LSB	2.44mV	4.88mV

Figure 3-7: Relationship between DI and AO

3.4 Digital Input and Output

To program the digital I/O operation is fairly straightforward. The digital input operation just reads data from its corresponding registers, and the digital output operation writes data to its corresponding registers. Note that the DIO data channel can only be read or written in the form of 16 bits. It is impossible to access individual bits.

The PCI-9111 provides 16 digital input and 16 digital output channels through CN1 and CN2. The digital I/O signals are fully TTL/DTL compatible. Detailed digital I/O signal specifications can be referred to in section 2.4.1.

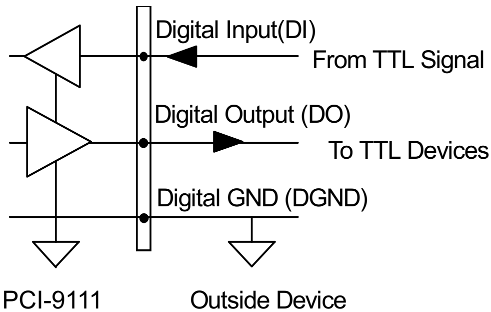

Figure 3-8: Digital Input and Output Circuit

3.5 Timer/Counter Operation

One programmable interval timer/counter chip is integrated on the PCI-9111. There are three counters available to the timer/counter chip and 6 possible operation modes for each counter. Figure 3-9 illustrates the block diagram of the timer/counter system.

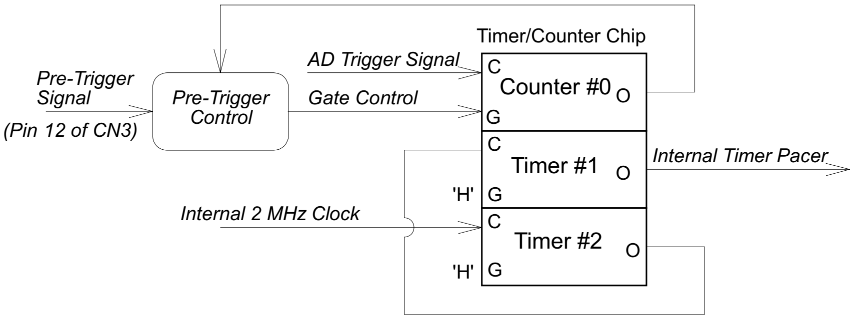

Figure 3-9: Timer/Counter Block Diagram

Pacer Trigger Source

Timers 1 and 2 are cascaded together to generate the timer pacer trigger for A/D conversion. The frequency of the pacer trigger is software controllable. The maximum pacer signal rate is 2MHz/4 = 500KHz which exceeds the maximum A/D conversion rate of the PCI-9111. The minimum signal rate is 2MHz/65535/65535, which is a very low frequency. Users are advised not to use it.

3.5.1 Pre-Trigger Counter

Timer #0 is used as a pre-trigger counter. The clock source of counter 0 is from the A/D trigger source so that the timer/counter can count the A/D trigger numbers after the pre-trigger signal (Pin 12 of CN3) is inserted. The gate control is set when the pre-trigger signal changes from ‘H’ to ‘L’, and is cleared when the counter counts down to zero. In the software library, timer #0 is always set as mode 0 (event counter).

Important Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil , pour éviter des blessures ou des dommages.

- Read these safety instructions carefully
- Keep the User's Manual for future reference
- Read the Specifications section of this manual for detailed information on the recommended operating environment
- The device can be operated at an ambient temperature of 50ºC
- When installing/mounting or uninstalling/removing device; or when removal of a chassis cover is required for user servicing:
  - Turn off power and unplug any power cords/cables
  - Reinstall all chassis covers before restoring power
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources
  - Keep device away from high heat or humidity
  - Keep device properly ventilated (do not block or cover ventilation openings)
  - Always use recommended voltage and power source settings
  - Always install and operate device near an easily accessible electrical outlet
  - Secure the power cord (do not place any object on/over the power cord)
  - Only install/attach and operate device on stable surfaces and/or recommended mountings
- If the device will not be used for long periods of time, turn off and unplug from its power source

- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools
- A Lithium-type battery may be provided for uninterrupted backup or emergency power.

CAUTION:

Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.
Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appro-priée.

- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged
  - Liquid has entered the device interior
  - The device has been exposed to high humidity and/or moisture
  - The device is not functioning or does not function according to the User's Manual
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefor, and any precautions required
  - Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location
- If PoE (Power over Ethernet) is enabled for the device, the system can ONLY be deployed indoors. Unless otherwise noted, the PoE system is NOT designed to withstand the rigors of outdoor use.

	**BURN HAZARD** Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching. ***RISQUE DE BRÛLURES*** *Ne touchez pas cette surface, cela pourrait entraîner des blessures.* *Pour éviter tout danger, laissez la surface refroidir avant de la toucher.*

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